

#### US009207909B1

### (12) United States Patent

### Langhammer

### (54) POLYNOMIAL CALCULATIONS OPTIMIZED FOR PROGRAMMABLE INTEGRATED CIRCUIT DEVICE STRUCTURES

(71) Applicant: Altera Corporation, San Jose, CA (US)

(72) Inventor: Martin Langhammer, Salisbury (GB)

(73) Assignee: Altera Corporation, San Jose, CA (US)

(\*) Notice: Subject to any disclaimer, the term of this

patent is extended or adjusted under 35

U.S.C. 154(b) by 267 days.

(21) Appl. No.: 13/790,106

(22) Filed: Mar. 8, 2013

### Related U.S. Application Data

- (60) Provisional application No. 61/729,797, filed on Nov. 26, 2012.
- (51) **Int. Cl. G06F** 7/**544** (2006.01)
- (52) **U.S. Cl.**

CPC ...... *G06F 7/5443* (2013.01)

(58) **Field of Classification Search**CPC combination set(s) only.
See application file for complete search history.

### (56) References Cited

### U.S. PATENT DOCUMENTS

3,473,160 A	10/1969	Wahlstrom
3,800,130 A	3/1974	Martinson et al
3,814,924 A	6/1974	Tate
3,896,299 A	7/1975	Rhodes
4,156,927 A	5/1979	McElroy et al.
4,179,746 A	12/1979	Tubbs
4,212,076 A	7/1980	Conners
4,215,406 A	7/1980	Gomola et al.
4,215,407 A	7/1980	Gomola et al.

### (10) Patent No.: US 9,207,909 B1 (45) Date of Patent: Dec. 8, 2015

4,422,155 A	12/1983	Amir et al.					
4,484,259 A	11/1984	Palmer et al.					
4,490,805 A *	12/1984	Tamura	708/603				
4,521,907 A	6/1985	Amir et al.					
4,575,812 A	3/1986	Kloker et al.					
4,597,053 A	6/1986	Chamberlin					
4,616,330 A	10/1986	Betz					
4,623,961 A	11/1986	Mackiewicz					
4,682,302 A	7/1987	Williams					
4,718,057 A	1/1988	Venkitakrishnan et al.					
4,727,508 A	2/1988	Williams					
4,736,335 A	4/1988	Barkan					
(Continued)							

### FOREIGN PATENT DOCUMENTS

EP	0 158 430	10/1985
EP	0 326 415	8/1989
	(Co	ntinued)

### OTHER PUBLICATIONS

Altera, "DSP Blocks in Stratix III Devices", Chapter 5, pp. 1-42, Mar. 2010.

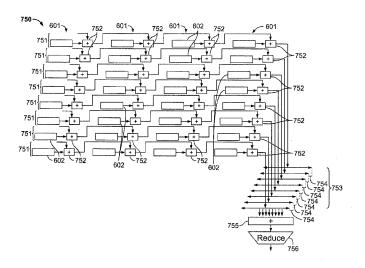
(Continued)

Primary Examiner — Chuong D Ngo Assistant Examiner — Calvin M Brien (74) Attorney, Agent, or Firm — Ropes & Gray LLP; Jeffrey H. Ingerman

### (57) ABSTRACT

Polynomial circuitry includes a respective partial product generator for each bit position of each term of a plurality of terms of a polynomial to be evaluated. A respective plurality of adders for each bit position adds partial products of a respective bit position across all of the plurality of terms to provide a respective bit-slice sum. Resulting bit-slice sums are offset from one another according to their respective bit positions. A final adder adds together the respective offset bit-slice sums to provide a result.

### 18 Claims, 8 Drawing Sheets



# US 9,207,909 B1 Page 2

(56) <b>Re</b> f	feren	ces Cited	5,644,519			Yatim et al.
II C DAT	ENIT	DOCUMENTS	5,644,522 5,646,545			Moyse et al. Trimberger et al.
U.S. FA1	EINI	DOCUMENTS	5,646,875			Taborn et al.
4,754,421 A 6/	1988	Bosshart	5,648,732	A		Duncan
4,777,614 A 10/	1988	Ward	5,652,903			Weng et al.
		Ku et al.	5,655,069 5,664,192			Ogawara et al. Lloyd et al.
		Mori Hedley et al.	5,689,195			Cliff et al.
		Mader	5,696,708		12/1997	
4,839,847 A 6/	1989	Laprade	5,729,495		3/1998 4/1998	Madurawe
4,871,930 A 10/	1989	Wong et al. Fujiyama	5,740,404 5,744,980			McGowan et al.
		Steele et al.	5,744,991			Jefferson et al.
		Morton	5,754,459			Telikepalli
, ,	1990		5,761,483 5,764,555			Trimberger McPherson et al.
	1990 1990	Quievy et al.  Duhamel et al 708/603	5,768,613			Asghar
	1991	Takeuchi et al.	5,771,186			Kodali et al.
		Hailey et al.	5,777,912 5,784,636		7/1998 7/1998	Leung et al.
	1991 1991	Martin et al. Turrini et al.	5,790,446			Yu et al.
		Thoen	5,794,067	Α	8/1998	Kadowaki
5,073,863 A 12/	1991	Zhang	5,801,546			Pierce et al.
		Tanaka	5,805,477 5,805,913		9/1998	Perner Guttag et al.
5,122,685 A 6/. 5,126,964 A * 6/.	1992 1002	Chan et al. Zurawski 708/625	5,808,926			Gorshtein et al.
		Steele	5,812,479			Cliff et al.
5,175,702 A 12/		Beraud et al.	5,812,562		9/1998	Baeg Dockser
		Ebeling et al. Freeman	5,815,422 5,821,776			McGowan
		Hsieh et al.	5,825,202			Tavana et al.
		Sutherland et al.	5,838,165		11/1998	
		Agarwala	5,841,684 5,847,579			Dockser Trimberger
	1994 1994	White New	5,847,978			Ogura et al.
		Jennings, III et al.	5,847,981			Kelley et al.
5,371,422 A 12/	1994	Patel et al.	5,859,878			Phillips et al. Bocchino
		Bearden et al.	5,869,979 5,872,380			Rostoker et al.
		Uramoto et al. Wedgwood et al.	5,874,834	A	2/1999	
5,404,324 A 4/	1995	Colon-Bonet	5,878,250			LeBlanc
		Dobbelaere et al.	5,880,981 5,892,962		3/1999 4/1999	Kojima et al. Cloutier
		Moyse et al. Jekel	5,894,228			Reddy et al.
5,452,231 A 9/		Butts et al.	5,898,602			Rothman et al.
		Rousseau et al.	5,931,898 5,942,914		8/1999 8/1999	
	1995	McCollum Goto	5,944,774	Α	8/1999	
	1995	Thepaut et al.	5,949,710			Pass et al.
	1996	Costello et al.	5,951,673 5,956,265		9/1999 9/1999	Miyata Lewis
	1996	Taylor Saishi et al.	5,959,871			Pierzchala et al.
		Doddington et al.	5,960,193			Guttag et al.
5,523,963 A 6/	1996	Hsieh et al.	5,961,635	A		Guttag et al.
		Pawate et al.	5,963,048 5,963,050			Harrison et al. Young et al.
		Kimura et al. Van Bavel et al.	5,968,196			Ramamurthy et al.
5,546,018 A 8/	1996	New et al.	5,970,254		10/1999	
		Ehlig et al.	5,978,260 5,982,195		11/1999	Trimberger et al. Cliff et al.
		Ngai et al. Hastings et al.	5,986,465		11/1999	
		Nelson	5,991,788		11/1999	Mintzer
		Oswald et al.	5,991,898 5,995,748		11/1999	Rajski et al. Guttag et al.
		Lytle et al. Lytle et al.	5,999,015			Cliff et al.
		Sansbury et al.	5,999,990	A	12/1999	Sharrit et al.
5,590,350 A 12/	1996	Guttag et al.	6,005,806	A	12/1999	
		Khong et al.	6,006,321 6,009,451		12/1999 12/1999	
		Brueckmann et al. Guttag et al.	6,018,755		1/2000	
		Pedersen	6,020,759	A	2/2000	Heile
		Adrian et al.	6,021,423			Nag et al.
		Behrens et al.	6,026,420 6,029,187			DesJardins et al. Verbauwhede
		Laczko et al. Nagaraj	6,031,763			Sansbury
		Okamoto	6,041,339		3/2000	Yu et al.
5,636,368 A 6/	1997	Harrison et al.	6,041,340	A	3/2000	Mintzer
5,640,578 A 6/	1997	Balmer et al.	6,052,327	Α	4/2000	Reddy et al.

# US 9,207,909 B1 Page 3

U.S. PATENT DOCUMENTS 6.09,375 A. 42000 Terrill et al. 6.052,755 A. 42000 Terrill et al. 6.052,755 A. 42000 Benovell et al. 6.052,376 B. 12000 Benovell et al. 6.072,396 A. 62000 Benovell et al. 6.073,156 A. 62000 Benovell et al. 6.073,156 A. 62000 Benovell et al. 6.073,157 B. 72000 Benovell et al. 6.083,177 A. 72000 Benovell et al. 6.083,177 A. 72000 Benovell et al. 6.093,167 A. 82000 Jenovell et al. 6.093,168 B. 12000 Jenovell et a	(56) Referen	nces Cited	6,591,283 B1		Conway et al.
6.052,755 A	IIS PATENT	DOCUMENTS	6,591,357 B2 6,600,495 B1		
Control   Cont	0.5. 17 HEIVI	DOCOMENTS			
Co055.555 A   42000   Doswell et al.   Co025.555 A   42000   Edwiner et al.   Co026.665,131 A   52000   Abbuving cal.   C725.441 Bl   42000   Keller et al.   C725.451 Bl   42000   Ke	6,052,755 A 4/2000	Terrill et al.			
Confect   A   52000   Condews et al   Confect   Confec					
Content					
6.069,487 A 5-2000 Pedersen 6.728,001 Bit 4.2004 Rajski et al. 6.009,487 A 5-2000 Pullips et al. 6.721,133 Bit 5.2004 Rosenberg 6.073,154 A 6-2000 Pullips et al. 6.721,234 Bit 5.2004 Rosenberg 6.073,154 A 6-2000 Pullips et al. 6.721,234 Bit 5.2004 Rosenberg 6.073,154 A 6-2000 Pullips et al. 6.721,234 Bit 5.2004 Rosenberg 6.073,154 Bit 5.2004 Rosenberg 6.074,154 Bit 5.20			6,725,441 B1	4/2004	Keller et al.
6072.994 A 62000 Dick	6,066,960 A 5/2000				
6.073,184 A 6.2000 Dick 6.734,278 B1 6.2004 Liu et al. 6.073,367 B2 7.2004 Kwon et al. 6.073,367 B2 7.2004 Kwon et al. 6.083,137 A 7.2006 Smith 6.711,094 B1 8.2004 Liu et al. 6.083,137 A 7.2006 Smith 6.711,094 B1 8.2004 Liu et al. 6.091,705 A 7.2009 Det Lange 6.734,066 B1 8.2004 Liu et al. 6.091,705 A 7.2009 Det Lange 6.734,066 B1 8.2004 Liu et al. 6.2004 Det al.					
6.073,381 A					
6.084,429 A 7,2000 Smith 6,781,048 Bl 8,2004 Langhammer et al. 6.081,317 A 7,2000 De Lange 6,784,669 Bl 8,2004 Line et al. 6.091,763 A 7,2000 De Lange 6,784,669 Bl 8,2004 Line et al. 6.091,763 A 7,2000 De Lange 6,784,669 Bl 8,2004 Line et al. 6.092,163 A 7,2000 Gonton et al. 6.093,163 A 8,2000 Gonton et al. 6.093,163 A 8,2000 Gonton et al. 6.093,163 A 8,2000 Gene et al. 6.107,820 A 8,2000 Gene et al. 6.107,821 A 8,2000 Redby et al. 6.107,821 A 8,2000 Redby et al. 6.107,824 A 8,2000 Redby et al. 6.107,824 A 8,2000 Redby et al. 6.107,824 A 10,2000 Robore et al. 6.107,824 A 11,2000 Robore et al. 6.107,824 Bl 10,2000 Robore et al. 6.107,825 Bl 10,2000 Robore et al. 6.107,824 Bl 10,2000 Robore et al. 6.107,825 Bl 10,200			6,745,254 B2		
6,091,261   A 7,2900   De Lange   G.774,669   Bl 8,2004   Liu et al.	6,084,429 A 7/2000	Trimberger			
Gold					
6.094,726 A 7,2000 Gonion et al. 6.093,163 A 8,2000 Unitag et al. 6.093,163 A 8,2000 Guitag et al. 6.0103,203 A 2,0000 Sulfage al. 6.0103,203 A 11,2000 Sulfage al. 6.0103,203 A 11					
6.099,163 A 8,2000 Guttag et al. 6801,234 B1 10,2004 Firenon et al. 6801,633 B1 10,2005 Firenon et al. 6801,633 B1 12,000 Firenon et al. 6901,7955 B1 7,2005 Firenon et al. 6901,7955 B1 1,2005			6,781,410 B2	8/2004	Pani et al.
6,107.820	6,097,988 A 8/2000				
6,107.821   A   8,2000   Redew et al.   6,836.839   B2   12,2004   Hosenauer   6,107.824   A   8,2000   Reddy et al.   6,874.079   B2   3,2005   Hosenauer   6,103.554   A   12,000   Kaviani et al.   6,944.71   B2   6,2005   Bogse et al.   6,144.980   A   11,2000   Oberman   6,917.955   B1   7,2005   Botchev   6,154.649   A   11,2000   Oberman   6,917.955   B1   7,2005   Botchev   6,154.649   A   11,2000   Oberman   6,917.955   B1   7,2005   Botchev   6,154.649   A   11,2000   Oberman   6,917.838   B1   11,2005   Turnigai et al.   6,163.788   A   12,2000   Chen et al.   6,978.287   B1   12,2005   Turnigai et al.   6,163.788   B1   12,001   Smith   6,983.300   B2   11,2005   Turnigai et al.   6,178.549   B1   12,001   Mirsky   7,024.446   B2   2,0006   Carvan   6,226.738   B1   5,2001   Mirsky   7,024.446   B2   2,0006   Carvan   6,243.729   B1   6,2001   Staszewski   7,062.556   B1   2,000   Maulik et al.   7,093.204   B2   8,2006   Chiernet al.   8,2006   Carvan   6,280.924   B1   2,000   Maulik et al.   7,107.305   B2   2,0006   Chiernet al.   6,280.924   B1   2,000   Maulik et al.   7,107.305   B2   2,0006   Chiernet al.   6,280.024   B1   2,000   Maulik et al.   7,107.305   B2   2,000   Chiernet al.   6,280.024   B1   2,000   Maulik et al.   7,113.909   B1   9,2000   Chiernet al.   6,237.608   B1   12,000   Page et al.   7,200.631   B2   4,2007   Mailsender et al.   6,331.455   B1   12,2001   Page et al.   7,331.585   B2   12,2007   Winternowd   2,300.808   B1   12,2001   Page et al.   7,331.585   B2   12,2007   Winternowd   6,353.443   B1   3,2002   Chabrazi et al.   7,413.585   B1   2,2002   Chabrazi et al.   7,413.656   B2   2,2008   Chabrazi et al.   7,413.656   B2   2,2008   Chabrazi et al.   7,413.656   B1   2,2002   Chabrazi et al.   7,413.656   B2   2,2008   Chabrazi et al.   7,413.656   B2   2,2008   Chabrazi et al.   7,413.					
6,107,824 A   8,2000   Roddy et al.   6,874,079   B2   3,2005   Hogenauer   6,130,554   A   10,2000   Kolze et al.   6,889,238   B2   5,2005   Sobnson   6,140,839   A   11,2000   New   6,924,663   B2   8,2005   Boggs et al.   6,151,4049   A   11,2000   New   6,924,663   B2   8,2005   Masui et al.   6,157,210   A   12,2000   Chen et al.   6,974,831   B1   2,0005   Long and et al.   6,167,418   A   12,2000   Chen et al.   6,978,287   B1   12,0005   Long and et al.   6,167,418   A   12,2000   Chen et al.   6,978,287   B1   12,0005   Long and et al.   6,173,849   B1   42,001   Smith   6,988,300   B2   12,000   Corava   6,173,849   B1   42,001   Smith   6,988,300   B2   12,000   Corava   6,242,347   B1   6,2001   Trinoberger   7,047,272   B2   8,2000   Glacalone et al.   6,243,729   B1   6,2001   Sinszwowiki   7,061,268   B1   6,2001   Lose   6,240,329   B1   6,2001   Sinszwowiki   7,061,268   B1   6,2000   Lose   6,240,328   B1   7,2001   Maulik et al.   7,032,204   B2   8,2000   Chem et al.   6,278,624   B1   9,2001   Vano et al.   7,1107,305   B2   9,2000   Chem et al.   6,314,542   B1   11,2001   Suruki   7,184,848   B2   2,2007   Striback et al.   6,314,543   B1   11,2001   Borland   7,200,631   B2   4,2007   Malanderer et al.   6,314,543   B1   11,2001   Borland   7,200,631   B2   4,2007   Malanderer et al.   6,323,680   B1   11,2001   Page et al.   7,334,888   B1   3,2000   Suruki   7,400,444   B1   1,2001   Roddy et al.   6,323,680   B1   11,2001   Page et al.   7,343,888   B1   3,2000   Suruki   4,2000   Roddy et al.   6,334,681   B1   12,2001   Chebraci et al.   7,434,888   B1   3,2000   Roddy et al.   6,335,343   B1   3,2002   Chebraci et al.   7,434,888   B1   3,2000   Roddy et al.   6,346,654   B1   2,2002   Abdott   7,448,860   B2   9,2008   Roddy et al.   6,353,468   B1   3,2002   Chebraci et al.   7,436,658   B2   9,2008   Sinit et al.   6,353,468   B1   3,2002   Chebraci et al.   7,436,658   B2   9,2008   Sinit et al.   6,353,632   B1   3,2002   Chebraci et al.   7,436,658   B2   9,2008   Sinit et					
6,140,839 A   10,200   Ravini et al.   6,904,471   B2   6,2005   Boggs et al.					
6,144,080   A   11/2000   Oberman   6,917,955   B1   77200   Solichev					
6,154,049   A   11/2000   New   6,924,663   B2   8,2005   Masui et al.	6,140,839 A 10/2000				
6,157,210 A 12/2000 Zaveri et al. 6,956,889 B3 11/2005 Dutta et al. 6,163,788 A 12/2000 Chen et al. 6,971,083 B1 11/2005 Imragia et al. 6,167,415 A 12/2000 Fischer et al. 6,971,083 B1 11/2005 Langhammer Fischer et al. 6,971,083 B1 11/2005 Langhammer Fischer et al. 6,971,083 B1 11/2005 Langhammer Fischer et al. 7,020,673 B2 3/2006 Ozawa G.226,735 B1 5/2001 Mirsky 7,024,446 B2 4/2006 Langhammer et al. 7,024,446 B1 4/2001 Jefferson et al. 7,024,446 B1 4/2001 Stazewski 7,061,268 B1 6/2001 Lesea 7,061,258 B1 6/2001 Lesea 7,061,258 B1 6/2001 Lesea 7,061,258 B1 6/2001 Lesea 7,062,526 B1 6/2001 Lesea 7,093,204 B1 6/2001 Maulik et al. 7,093,204 B1 6/2001 Maulik et al. 7,093,204 B1 6/2001 Vano et al. 7,107,305 B2 9,2006 Ottem et al. 6,279,021 B1 8/2001 Takano et al. 7,107,305 B2 9,2006 Green et al. 6,314,442 B1 11/2001 Surzuki 7,181,484 B2 2/2007 Striback et al. 6,314,451 B1 11/2001 Borland 7,206,318 B1 2/2006 Green et al. 6,314,451 B1 11/2001 Borland 7,206,318 B1 2/2007 Mailaender et al. 6,321,466 B1 11/2001 Pedersen et al. 7,331,358 B1 2/2007 Mailaender et al. 6,323,608 B1 11/2001 Pedersen et al. 7,331,358 B1 2/2007 Mailaender et al. 6,364,648 B1 2/2002 New 7,395,298 B1 2/2001 Arakawa et al. 7,345,388 B1 3/2008 Burney et al. 6,363,448 B1 2/2002 New 7,395,298 B1 2/2001 Arakawa et al. 7,404,417 B2 2/2003 Debes et al. 6,363,448 B1 2/2002 Debes et al. 7,404,417 B2 2/2003 Debes et al. 6,360,448 B1 3/2002 Deak et al. 7,425,656 B2 9/2008 Siu et al. 6,360,448 B1 4/2002 Davis 7,404,417 B1 9/2005 Roce et al. 6,360,448 B1 4/2002 Davis 7,404,417 B1 9/2005 Roce et al. 6,360,448 B1 4/2002 Davis 7,404,417 B1 9/2005 Roce et al. 6,360,448 B1 4/2002 Davis 7,404,417 B1 9/2005 Roce et al. 6,360,448 B1 4/2002 Davis 7,404,417 B1 9/2005 Roce et al. 6,360,448 B1 4/2002 Davis 7,404,417 B1 9/2005 Roce et al. 6,360,448 B1 4/2002 Davis 7,404,417 B1 9/2005 Roce et al. 6,360,448 B1 4/2002 Davis 6 All 4,404 B1 6/2002 Davis 6 All 4,404 B1 6	6.154.049 A 11/2000		6,924,663 B2		
167.415 A   12/200   Fischer et al.   6.978.287 Bl   12/200   Langhammer   6.167.415 A   12/200   Smith   6.983.300 Bz   1/2006   Czawa   6.215.326 Bl   4/200   Jefferson et al.   7.020.673 Bz   3/2006   Czawa   6.226,747 Bl   5/2001   Trimberger   7.04.747 Bz   5/2006   Giacalone et al.   6.242.947 Bl   6/2001   Smith   7.020.673 Bz   5/2006   Giacalone et al.   6.242.947 Bl   6/2001   Smith   6/2005   Cawa   6/2004   Cawa					
Color					
C.215.326   BI   42001   Idfarson et al.   7.020.673   BZ   3/2006   Czawa   C.226.738   BI   5/2001   Mirsky   7.047.272   BZ   5/2006   C.243.729   BI   6/2001   Trimberger   7.047.272   BZ   5/2006   C.243.729   BI   6/2001   C.2001   Trimberger   7.047.272   BZ   5/2006   C.263.729   C.243.729   BI   6/2001   C.2001   C.263.828   C.2001   C.2001   C.263.828   C.2001   C.20					
6.226,735 Bl 5/2001 Minsky 7,024,446 BJ 4/2006 Langhammer et al. 6.2426,729 Bl 6/2001 Timberger 7,047,272 BJ 5/2006 Cleet al. 326/39 6.246,248,729 Bl 6/2001 Lesen 7,061,268 Bl 6/2006 Cleet al. 326/39 6.246,258 Bl 6/2001 Lesen 7,062,256 Bl 6/2006 Cleet al. 326/39 6.266,053 Bl 7/2001 Maulik et al. 7,093,204 BJ 8/2006 Cleet al. 326/39 6.269,053 Bl 7/2001 Maulik et al. 7,107,305 BJ 2/2006 Cleet al. 326/39 6.269,053 Bl 7/2001 Maulik et al. 7,107,305 BJ 2/2006 Cleen et al. 6.286,024 Bl 9/2001 Yano et al. 7,113,969 Bl 9/2006 Green et al. 7,113,451 Bl 11/2001 Borland 7,230,451 Bl 6/2007 Mailander et al. 8,114,551 Bl 11/2001 Page et al. 7,230,451 Bl 6/2007 Mailander et al. 8,114,551 Bl 11/2001 Page et al. 7,313,585 BJ 12/2007 Winterrowd G.323,680 Bl 11/2001 Pedersen et al. 7,313,585 BJ 12/2007 Winterrowd G.323,680 Bl 11/2001 Pedersen et al. 7,343,388 Bl 3/200 Pedersen et al. 7,355,298 BJ 2/2007 Winterrowd G.334,683 Bl 3/2002 New 7,395,298 BJ 2/2007 Winterrowd G.353,468 Bl 3/2002 Cleehrazi et al. 7,409,417 BJ 2/2008 Flyimori G.366,050 Bl 3/2002 Takano et al. 7,409,418 Bl 2/2008 Flyimori G.366,050 Bl 3/2002 Takano et al. 7,409,418 Bl 2/2008 Flyimori G.366,050 Bl 3/2002 Flower et al. 7,409,418 Bl 2/2008 Flyimori G.366,050 Bl 4/2002 Davis Takano et al. 7,409,418 Bl 2/2008 Flyimori G.368,050 Bl 2			7,020,673 B2		
C.246,275 B1   62001   Staszewski   7,061,268 B1   6,0006   Hoyle	6,226,735 B1 5/2001	Mirsky			
C.246,258 Bl   6200   Lesea   T.200   Lesea   T.200   C.260,033 Bl   7200   Lesea   T.200   C.260,033 Bl   7200   Takano et al.   T.107,305 Bz   92006   Oktem et al.	6,242,947 B1 6/2001				
6.260,053 Bl 7/2001 Maulik et al. 7,093,204 Bl 8,2006 Oktem et al. 6.279,021 Bl 8,2001 Takano et al. 7,107,305 Bl 9/2006 Deng et al. 6.286,024 Bl 9/2001 Yano et al. 7,113,969 Bl 9/2006 Deng et al. 6.314,442 Bl 11/2001 Borland 7,200,631 Bl 4/2007 Mailaender et al. 7,200,631 Bl 11/2001 Borland 7,200,631 Bl 6/2007 Langhammer 6,321,246 Bl 11/2001 Pedersen et al. 7,230,451 Bl 6/2007 Langhammer 7,200,631 Bl 6/2007 Langhammer 7,200,631 Bl 6/2007 Langhammer 8,321,246 Bl 11/2001 Pedersen et al. 7,313,585 Bl 11/2001 Pedersen et al. 7,313,585 Bl 1/2001 Pedersen et al. 7,343,388 Bl 3/2008 Bl 1/2002 Per Pedersen et al. 7,401,109 Bl 7/2008 Koc et al. 8,354,486 Bl 2/2002 Per Pedersen et al. 7,401,109 Bl 7/2008 Koc et al. 8,354,486 Bl 3/2002 Per Pedersen et al. 7,415,442 Bl 8/2008 Lou Pedersen et al. 7,415,442 Bl 8/2008 Lou Pedersen et al. 7,415,442 Bl 8/2008 Lou Pedersen et al. 7,415,445 Bl 9/2008 Rarick et al. 8,354,445 Bl 1/2002 Per Pedersen et al. 7,428,456 Bl 9/2008 Superber et al. 8,366,401 Bl 4/2002 Davis 7,430,578 Bl 9/2008 Superber et al. 8,366,401 Bl 4/2002 Davis 7,430,578 Bl 9/2008 Superber et al. 8,366,401,576 Bl 6/2002 Pedersen et al. 7,428,456 Bl 9/2008 Superber et al. 8,366,401,576 Bl 6/2002 Pedersen et al. 7,536,430 Bl 1/2008 Koc et al. 8,366,401,576 Bl 6/2002 Pedersen et al. 7,536,430 Bl 1/2008 Simkins et al. 8,447,578 Bl 8/2002 Helle 7,506,676 Bl 9/2009 Pedersen et al. 8,366,401,576 Bl 6/2009 Pedersen et al. 7,506,676 Bl 9/2009 Pedersen et al. 8,366,401,401 Bl 9/2009 Pedersen et al. 8,366,401,401 Bl 9/2009 Pedersen et al. 8,366,401,401 Bl 1/2001 Pedersen et al. 8,366,401,401 Bl 9/2002 Pedersen et al. 8,366,401,401 Bl 1/2001 Pedersen et al. 8,366,401,401 Bl 9/2002 Pedersen et al. 8,366,401,401 Bl 9/2009 Pedersen					
6,279,021 BI 8/2001 Takano et al. 7,110,305 B2 9/2006 Green et al. 6,279,024 BI 9/2006 Green et al. 6,279,024 BI 1/2001 Suzuki 7,181,484 B2 2/2007 Green et al. 6,314,442 BI 1/2001 Borland 7,200,631 B2 4/2007 Mailaender et al. 6,321,246 BI 1/2001 Pedersen et al. 7,230,451 BI 6/2007 Mailaender et al. 6,321,246 BI 1/2001 Pedersen et al. 7,313,588 B2 1/2007 Winterrowd 6,323,680 BI 11/2001 Pedersen et al. 7,313,588 B1 3/2008 BI 11/2001 Arakawa et al. 7,343,388 B1 3/2008 Burney et al. 6,346,824 BI 2/2002 Abbott 7,401,109 B2 7/2008 Debes et al. 6,351,843 BI 3/2002 Chehrazi et al. 7,409,417 B2 8/2008 Lou 6,353,843 BI 3/2002 Park et al. 7,415,424 B2 8/2008 Hennedy et al. 6,360,240 BI 3/2002 Park et al. 7,415,424 B2 8/2008 Hennedy et al. 6,360,240 BI 3/2002 Park et al. 7,415,425 B2 8/2008 Hennedy et al. 6,366,944 BI 4/2002 Hossain et al. 7,428,566 B2 9/2008 Siu et al. 6,367,031 BI 4/2002 Davis 7,430,678 B2 9/2008 Siu et al. 6,367,031 BI 4/2002 Davis 7,430,678 B2 9/2008 Debes et al. 6,377,970 BI 4/2002 Davis 7,430,678 B2 9/2008 Debes et al. 6,377,970 BI 4/2002 Cheung et al. 7,472,155 B2 1/2008 Sopeher et al. 6,407,576 BI 6/2002 Cw et al. 7,536,430 B2 5/2009 Ginevokian et al. 6,407,576 BI 6/2002 Cw et al. 7,536,430 B2 5/2009 Ginevokian et al. 6,407,576 BI 6/2002 Cw et al. 7,536,430 B2 5/2009 Euglimori 6,438,569 BI 8/2002 Choung et al. 7,536,430 B2 5/2009 Euglimori 6,438,569 BI 8/2002 Choung et al. 7,536,430 B2 5/2009 Euglimori 6,438,569 BI 8/2002 Choung et al. 7,536,430 B2 1/2008 Cover et al. 6,438,569 BI 8/2002 Choung et al. 7,536,430 B2 1/2000 Euglian et al. 6,438,569 BI 8/2002 Choung et al. 7,536,430 B2 1/2000 Euglian et al. 6,438,569 BI 8/2002 Euglian et al. 7,536,430 B2 1/2000 Euglian et al. 6,438,569 BI 8/2002 Choung et al. 7,536,430 B2 1/2000 Euglian et al. 6,438,569 BI 8/2002 Choung et al. 7,536,430 B2 1/2000 Euglian et al. 6,438,569 BI 8/2002 Euglian et al. 7,536,430 B2 1/2001 Euglian et al. 6,438,569 BI 8/2002 Euglian et al. 7,536,430 B2 1/2001 Euglian et al. 6,438,569 BI 8/2002 Euglian et al. 7,536,430 B2 1/2001					
Company	6,279,021 B1 8/2001				
11/200					
6.321,246 B1         11/2001         Page et al.         7,230,451 B1         620207         Langhammer           6.327,605 B2         12/2001         Arakawa et al.         7,343,388 B1         3/2008 Burney et al.           6,346,828 B1         22002         New         7,343,388 B1         3/2008 Burney et al.           6,351,142 B1         22002         New         7,401,109 B2         7/2008 Debes et al.           6,353,843 B1         3/2002 Park et al.         7,401,109 B2         7/2008 Debes et al.           6,350,246 B1         3/2002 Park et al.         7,415,542 B2         8/2008 Lou           6,360,240 B1         3/2002 Park et al.         7,421,656 B1         9/2008 Rarick et al.           6,360,60 B1         3/2002 Park et al.         7,428,566 B2         9/2008 Rarick et al.           6,360,610 B1         4/2002 Hossain et al.         7,430,578 B2         9/2008 Siu et al.           6,367,003 B1         4/2002 Hossain et al.         7,430,578 B2         9/2008 Sperber et al.           6,377,970 B1         4/2002 Cheung et al.         7,430,578 B2         9/2008 Sperber et al.           6,407,576 B1         6/2002 Coe et al.         7,536,393 B2         3/2009 Sperber et al.           6,407,694 B1         6/2002 Mgai et al.         7,536,430 B2         2/2008 Simkins et al.			7,200,631 B2	4/2007	Mailaender et al.
Care	6,321,246 B1 11/2001	Page et al.			
Color					
6,351,142 B1 2/2002 Abbott 7,401,109 B2 7/2008 Koe et al. 6,353,843 B1 3/2002 Chehrazi et al. 7,415,542 B2 8/2008 Lou 6,359,468 B1 3/2002 Takano et al. 7,415,542 B2 8/2008 Hennedy et al. 6,360,240 B1 3/2002 Takano et al. 7,421,465 B1 9/2008 Fujimori 6,366,944 B1 4/2002 Hossain et al. 7,428,566 B2 9/2008 Fujimori 6,366,944 B1 4/2002 Davis 7,430,578 B2 9/2008 Uct al. 6,367,003 B1 4/2002 Davis 7,430,578 B2 9/2008 Debes et al. 6,369,610 B1 4/2002 Cheung et al. 7,430,656 B2 9/2008 Sperber et al. 6,377,970 B1 4/2002 Abdallah et al. 7,447,310 B2 11/2008 Coe et al. 6,385,632 B1 5/2002 Choe et al. 7,472,155 B2 12/2008 Simkins et al. 6,407,576 B1 6/2002 Cox et al. 7,508,936 B2 3/2009 Eberle et al. 6,407,694 B1 6/2002 Cox et al. 7,536,430 B2 5/2009 Guevokian et al. 6,427,157 B1 7/2002 Webb 7,567,997 B2 7/2009 Simkins et al. 6,434,587 B1 8/2002 Liao et al. 7,590,676 B1 9/2009 Eberle et al. 6,438,570 B1 8/2002 Liao et al. 7,590,676 B1 9/2009 DB Brown Elliott et al. 6,438,570 B1 8/2002 Knowles 7,719,446 B2 2/2010 DB Rown Elliott et al. 6,438,382 B1 9/2002 Knowles 7,719,446 B2 5/2010 Brown Elliott et al. 6,467,017 B1 10/2002 Koe 7,720,888 B2 5/2010 Grown et al. 6,483,343 B1 11/2002 Spai et al. 7,769,797 B2 8/2010 Driker et al. 6,483,343 B1 11/2002 Faith et al. 7,769,797 B2 8/2010 Uverma et al. 6,483,343 B1 11/2002 Faith et al. 7,885,541 B1 10/2010 Verma et al. 6,531,888 B2 3/2003 Abbott 7,917,567 B1 10/2010 Verma et al. 6,531,888 B2 3/2003 Black et al. 7,930,336 B2 4/2011 Langhammer et al. 6,531,888 B2 3/2003 Giacalone et al. 7,930,336 B2 4/2011 Langhammer et al. 6,557,029 B1 4/2003 Giacalone et al. 8,041,759 B1 10/2011 Langhammer et al. 6,571,768 B1 5/2003 Giacalone et al. 8,041,759 B1 10/2011 Shimanek et al. 6,571,768 B1 6/2003 Karimi et al. 8,090,758 B1 1/2012 Shimanek et al.					
Section   Sect					
Color					
6,362,650 B1 3/2002 New et al. 7,428,565 B2 9/2008 Fujimori 6,366,944 B1 4/2002 Hossain et al. 7,428,565 B2 9/2008 Siu et al. 9/2008 Obes et al. 7,430,678 B2 9/2008 Siu et al. 9/2008 Debes et al. 9/2009 Debes et al. 9/2008 Debes et al. 9/2009 Debes					
6,366,944 B1 4/2002 Davis 7,438,566 B2 9/2008 Sit et al. 6,367,003 B1 4/2002 Davis 7,430,656 B2 9/2008 Debes et al. 6,367,003 B1 4/2002 Cheung et al. 7,430,656 B2 9/2008 Sperber et al. 6,377,970 B1 4/2002 Abdallah et al. 7,447,310 B2 11/2008 Koc et al. 6,385,632 B1 5/2002 Choe et al. 7,472,155 B2 12/2008 Simkins et al. 6,407,576 B1 6/2002 Ngai et al. 7,536,936 B2 3/2009 Eberle et al. 6,407,694 B1 6/2002 Cox et al. 7,536,430 B2 5/2009 Guevokian et al. 6,407,694 B1 6/2002 Cox et al. 7,536,430 B2 5/2009 Guevokian et al. 6,427,157 B1 7/2002 Webb 7,567,997 B2 7/2009 Simkins et al. 6,434,887 B1 8/2002 Liao et al. 7,590,676 B1 9/2009 Langhammer 6,438,560 B1 8/2002 Abbott 7,646,430 B2 1/2010 Brown Elliott et al. 6,438,570 B1 8/2002 Miller 7,668,896 B2 2/2010 Lutz et al. 6,436,171 B1 10/2002 Heile 7,720,898 B2 5/2010 Driker et al. 6,467,017 B1 10/2002 Ngai et al. 7,769,797 B2 8/2010 Cho et al. 6,480,980 B2 11/2002 Koe 7,814,136 B1 10/2010 Mauer 6,483,343 B1 11/2002 Faith et al. 7,814,137 B1 10/2010 Mauer 6,483,343 B1 11/2002 Faith et al. 7,836,117 B1 11/2010 Langhammer et al. 6,523,055 B1 2/2003 Savo et al. 7,836,117 B1 11/2011 Langhammer 6,531,888 B2 3/2003 Abbott 7,917,567 B1 3/2011 Mason et al. 6,533,870 B1 3/2003 Langhammer et al. 7,930,335 B2 4/2011 Gura 6,542,000 B1 4/2003 Langhammer et al. 7,930,336 B2 4/2011 Mason et al. 6,557,092 B1 4/2003 Callen 7,974,997 B2 7/2011 Neoh et al. 6,573,749 B2 6/2003 Karimi et al. 8,041,759 B1 10/2011 Langhammer et al. 6,573,749 B2 6/2003 Karimi et al. 8,041,759 B1 10/2011 Langhammer et al. 6,573,740 B1 6/2003 Karimi et al. 8,041,759 B1 10/2011 Langhammer et al. 6,573,740 B1 6/2003 Karimi et al. 8,041,759 B1 10/2011 Langhammer et al.			7,428,565 B2		
6,369,610 B1 4/2002 Cheung et al. 7,430,656 B2 9/2008 Sperber et al. 6,377,970 B1 4/2002 Abdallah et al. 7,4472,155 B2 1/2008 Simkins et al. 5/2002 Choe et al. 7,472,155 B2 1/2008 Simkins et al. 5/2005 Choe et al. 7,508,936 B2 1/2009 Eberle et al. 6/207,676 B1 6/2002 Cox et al. 7,536,430 B2 5/2009 Eberle et al. 6/207,694 B1 6/2002 Cox et al. 7,536,430 B2 5/2009 Simkins et al. 6/27,157 B1 7/2002 Webb 7,567,997 B2 7/2009 Simkins et al. 6/27,157 B1 7/2002 Webb 7,567,997 B2 7/2009 Simkins et al. 6/23,587 B1 8/2002 Liao et al. 7,590,676 B1 9/2009 Langhammer 6/23,856 B1 8/2002 Abbott 7,646,430 B2 1/2010 Brown Elliott et al. 6/23,8570 B1 8/2002 Miller 7,668,896 B2 2/2010 Lutz et al. 6/245,3382 B1 9/2002 Knowles 7,719,446 B2 5/2010 Brown Elliott et al. 6/253,382 B1 9/2002 Heile 7,720,898 B2 5/2010 Driker et al. 6/267,017 B1 10/2002 Ngai et al. 7,769,797 B2 8/2010 Cho et al. 6/203,343 B1 11/2002 Koe 7,814,136 B1 10/2010 Verma et al. 6/23,343 B1 11/2002 Faith et al. 7,814,137 B1 10/2010 Mauer 6/23,055 B1 2/2003 Yu et al. 7,827,799 B1 10/2010 Langhammer et al. 6/523,055 B1 2/2003 Savo et al. 7,865,541 B1 1/2011 Langhammer 6/23,388 B2 3/2003 Abbott 7,917,567 B1 3/2011 Mason et al. 6/203 Karimi et al. 7,930,336 B2 4/2011 Langhammer 6/2556,044 B2 4/2003 Langhammer et al. 7,949,699 B1 5/2011 Langhammer 6/2556,044 B2 4/2003 Callen 7,949,699 B1 5/2011 Langhammer et al. 6/2573,749 B2 6/2003 New et al. 8,090,758 B1 1/2012 Shimanek et al. 6/2574,762 B1 6/2003 Karimi et al. 8,090,758 B1 1/2015 Shimanek et al. 6/2574,762 B1 6/2003 Karimi et al. 8,090,758 B1 1/2015 Shimanek et al.	6,366,944 B1 4/2002				
6,377,970 B1 4/2002 Abdallah et al. 7,447,310 B2 11/2008 Koc et al. 6,385,632 B1 5/2002 Choe et al. 7,472,155 B2 12/2008 Simkins et al. 7,508,936 B2 3/2009 Eberle et al. 7,536,430 B2 5/2009 Guevokian et al. 7,536,430 B2 5/2009 Simkins et al. 8,427,157 B1 7/2002 Webb 7,567,997 B2 7/2009 Simkins et al. 8,434,587 B1 8/2002 Liao et al. 7,590,676 B1 9/2009 Langhammer et al. 6,434,587 B1 8/2002 Miller 7,664,430 B2 1/2010 Brown Elliott et al. 8/208,509 B1 8/2002 Miller 7,668,896 B2 2/2010 Lutz et al. 8/20,438,570 B1 8/2002 Miller 7,668,896 B2 2/2010 Rown Elliott et al. 8/20,438,570 B1 8/2002 Miller 7,720,898 B2 5/2010 Rosenthal et al. 8/20,446,107 B1 9/2002 Knowles 7,719,446 B2 5/2010 Rosenthal et al. 8/20,446,107 B1 9/2002 Mgai et al. 7,720,898 B2 5/2010 Driker et al. 8/20,446,107 B1 10/2002 Ngai et al. 7,769,797 B2 8/2010 Cho et al. 8/20,480,980 B2 11/2002 Koe 7,814,136 B1 10/2010 Verma et al. 8/20,487,575 B1 11/2002 Faith et al. 7,814,137 B1 10/2010 Mauer 6,487,575 B1 11/2002 Oberman 7,822,799 B1 10/2010 Langhammer et al. 8/23,055 B1 2/2003 Savo et al. 7,836,117 B1 11/2011 Langhammer et al. 8/23,058 B1 2/2003 Savo et al. 7,917,567 B1 3/2011 Langhammer et al. 8/23,058,470 B1 3/2003 Langhammer et al. 7,930,335 B2 4/2011 Choa et al. 8/24,000 B1 4/2003 Black et al. 7,930,335 B2 4/2011 Langhammer et al. 8/25,050,000 B1 4/2003 Black et al. 7,930,335 B2 4/2011 Langhammer et al. 8/257,092 B1 4/2003 Callen 7,974,997 B2 7/2011 Langhammer et al. 8/257,092 B1 4/2003 Callen 7,974,997 B2 7/2011 Langhammer et al. 8/257,092 B1 4/2003 Callen 7,974,997 B2 7/2011 Langhammer et al. 8/257,092 B1 4/2003 Callen 7,974,997 B2 7/2011 Langhammer et al. 8/257,092 B1 4/2003 Karimi et al. 8/2010 Savore et al. 8/2010 Siminanek et al.					
6,385,632 B1 5/2002 Choe et al. 7,472,155 B2 12/2008 Simkins et al. 6,407,576 B1 6/2002 Ngai et al. 7,508,936 B2 5/2009 Guevokian et al. 5/2000 Guevokian et al. 5/2009 Guevokian et al. 5/2000 Guevokian et al. 5/2001 Guevokian et al. 5/2001 Guevokian et al. 5/2001 Guevokian et al. 5/2001 Guevokian et al. 5/2000 Guevokian et al. 5/2001 Guevok	6,369,610 B1 4/2002 6,377,970 B1 4/2002	Cheung et al. Abdallah et al			
6,407,694 B1 6/2002 Cox et al. 7,536,430 B2 5/2009 Guevokian et al. 6,427,157 B1 7/2002 Webb 7,567,997 B2 7/2009 Simkins et al. 1. 7,504,436,87 B1 8/2002 Liao et al. 7,590,676 B1 9/2009 Langhammer et al. 6,434,587 B1 8/2002 Abbott 7,668,896 B2 1/2010 Brown Elliott et al. 6,438,570 B1 8/2002 Miller 7,668,896 B2 2/2010 Lutz et al. 6,446,107 B1 9/2002 Knowles 7,719,446 B2 5/2010 Rosenthal et al. 6,453,382 B1 9/2002 Heile 7,720,898 B2 5/2010 Driker et al. 6,467,017 B1 10/2002 Ngai et al. 7,769,797 B2 8/2010 Oriker et al. 6,480,980 B2 11/2002 Koe 7,814,136 B1 10/2010 Verma et al. 6,483,343 B1 11/2002 Faith et al. 7,814,137 B1 10/2010 Mauer 6,487,575 B1 11/2002 Oberman 7,822,799 B1 10/2010 Langhammer et al. 6,523,057 B1 2/2003 Yu et al. 7,864,117 B1 11/2010 Langhammer et al. 6,531,888 B2 3/2003 Abbott 7,917,567 B1 3/2011 Langhammer et al. 6,538,470 B1 3/2003 Langhammer et al. 7,930,335 B2 4/2011 Gura 6,554,000 B1 4/2003 Black et al. 7,930,336 B2 4/2011 Langhammer et al. 6,557,042 B1 4/2003 Glacalone et al. 8,090,758 B1 1/2012 Shimanck et al. 8,090,758 B1 1/2012 Shimanck et al. 6,573,749 B2 6/2003 New et al. 8,090,758 B1 1/2012 Shimanck et al. 8,112,466 B2 2/2012 Minz et al.					
6,427,157 B1 7/2002 Webb 7,567,997 B2 7/2009 Simkins et al. 6,434,587 B1 8/2002 Liao et al. 7,590,676 B1 9/2009 Langhammer 6,438,559 B1 8/2002 Abbott 7,646,430 B2 1/2010 Brown Elliott et al. 6,438,559 B1 8/2002 Knowles 7,668,896 B2 2/2010 Lutz et al. 6,446,107 B1 9/2002 Knowles 7,719,446 B2 5/2010 Rosenthal et al. 6,453,382 B1 9/2002 Heile 7,720,898 B2 5/2010 Driker et al. 6,467,017 B1 10/2002 Ngai et al. 7,769,797 B2 8/2010 Cho et al. 6,483,343 B1 11/2002 Faith et al. 7,814,136 B1 10/2010 Verma et al. 6,487,575 B1 11/2002 Oberman 7,822,799 B1 10/2010 Langhammer et al. 6,523,055 B1 2/2003 Yu et al. 7,836,117 B1 11/2010 Langhammer et al. 6,531,888 B2 3/2003 Abbott 7,917,567 B1 3/2011 Mason et al. 6,538,470 B1 3/2003 Langhammer et al. 7,930,335 B2 4/2011 Langhammer 6,556,044 B2 4/2003 Langhammer et al. 7,930,336 B2 4/2011 Langhammer 6,571,268 B1 5/2003 New et al. 8,041,759 B1 10/2011 Langhammer 6,573,749 B2 6/2003 New et al. 8,090,758 B1 1/2012 Shimanek et al. 8,041,759 B1 10/2011 Langhammer et al. 8,041,759 B1 10/2011 Langhammer 8,794,969 B1 5/2011 Neoh et al. 8,041,759 B1 10/2011 Langhammer 8,794,969 B1 5/2011 Langhammer 8,794,969 B1 5/2011 Langhammer 8,794,969 B1 5/2011 Langhammer 8,794,969 B1 10/2011 Langhammer 8,794,969 B1 5/2011 Langhammer 8,794,969 B1 5/2011 Langhammer 8,794,969 B1 5/2011 Langhammer 8,794,969 B1 5/2011 Langhammer et al. 8,041,759 B1 10/2011 Langhammer et al.					
6,434,587 B1 8/2002 Liao et al. 7,590,676 B1 9/2009 Langhammer 6,438,569 B1 8/2002 Abbott 7,646,430 B2 1/2010 Brown Elliott et al. 7,646,430 B2 1/2010 Lutz et al. 8/2002 Miller 7,668,896 B2 2/2010 Lutz et al. 8/2002 Miller 7,719,446 B2 5/2010 Driker et al. 8/2010 Priker et al. 8/2010 Priker et al. 8/2010 Priker et al. 8/2010 Priker et al. 8/2010 Cho et al. 8/2010 Cho et al. 8/2010 Priker et al. 8/2010 Pri					
6,438,569 B1			7,590,676 B1		
6,446,107 B1 9/2002 Knowles 7,719,446 B2 5/2010 Rosenthal et al. 6,4453,382 B1 9/2002 Heile 7,720,898 B2 5/2010 Driker et al. 6,467,017 B1 10/2002 Ngai et al. 7,769,797 B2 8/2010 Cho et al. 6,480,980 B2 11/2002 Koe 7,814,136 B1 10/2010 Verma et al. 6,483,343 B1 11/2002 Faith et al. 7,814,137 B1 10/2010 Mauer 6,487,575 B1 11/2002 Oberman 7,822,799 B1 10/2010 Langhammer et al. 6,523,055 B1 2/2003 Yu et al. 7,836,117 B1 11/2010 Langhammer et al. 6,523,057 B1 2/2003 Savo et al. 7,865,541 B1 1/2011 Langhammer 6,531,888 B2 3/2003 Abbott 7,917,567 B1 3/2011 Mason et al. 6,538,470 B1 3/2003 Langhammer et al. 7,930,335 B2 4/2011 Gura 6,542,000 B1 4/2003 Black et al. 7,930,336 B2 4/2011 Gura 6,557,092 B1 4/2003 Callen 7,974,997 B2 7/2011 Langhammer 6,557,092 B1 4/2003 Giacalone et al. 8,041,759 B1 10/2011 Langhammer et al. 6,573,749 B2 6/2003 Karimi et al. 8,090,758 B1 1/2012 Shimanek et al. 6,574,762 B1 6/2003 Karimi et al. 8,112,466 B2 2/2012 Minz et al.	6,438,569 B1 8/2002				
6,453,382 B1 9/2002 Heile 7,720,898 B2 5/2010 Driker et al. 6,467,017 B1 10/2002 Ngai et al. 7,769,797 B2 8/2010 Cho et al. 6,480,980 B2 11/2002 Koe 7,814,136 B1 10/2010 Verma et al. 6,483,343 B1 11/2002 Faith et al. 7,814,137 B1 10/2010 Mauer 6,487,575 B1 11/2002 Oberman 7,822,799 B1 10/2010 Langhammer et al. 6,523,055 B1 2/2003 Yu et al. 7,836,117 B1 11/2010 Langhammer et al. 6,523,057 B1 2/2003 Savo et al. 7,865,541 B1 1/2011 Langhammer 6,531,888 B2 3/2003 Abbott 7,917,567 B1 3/2011 Mason et al. 6,538,470 B1 3/2003 Langhammer et al. 7,930,335 B2 4/2011 Gura 6,542,000 B1 4/2003 Black et al. 7,930,336 B2 4/2011 Langhammer 6,556,044 B2 4/2003 Langhammer et al. 7,949,699 B1 5/2011 Neoh et al. 6,577,092 B1 4/2003 Giacalone et al. 8,041,759 B1 10/2011 Langhammer et al. 6,573,749 B2 6/2003 New et al. 8,090,758 B1 1/2012 Shimanek et al. 6,574,762 B1 6/2003 Karimi et al. 8,112,466 B2 2/2012 Minz et al.					
6,467,017 B1 10/2002 Ngai et al. 7,769,797 B2 8/2010 Cho et al. 6,480,980 B2 11/2002 Koe 7,814,136 B1 10/2010 Verma et al. 10/2010 Mauer (6,483,343 B1 11/2002 Faith et al. 7,814,137 B1 10/2010 Langhammer et al. 10/2010 Langhammer et al. 10/2010 Langhammer et al. 10/2030 Yu et al. 7,836,117 B1 11/2010 Langhammer et al. 11/2030 Savo et al. 7,865,541 B1 11/2011 Langhammer et al. 11/2031 Shimanek et al. 11/20			7,720,898 B2		
6,483,343 B1 11/2002 Faith et al. 7,814,137 B1 10/2010 Mauer (6,487,575 B1 11/2002 Oberman 7,822,799 B1 10/2010 Langhammer et al. (6,523,055 B1 2/2003 Yu et al. 7,836,117 B1 11/2010 Langhammer et al. (6,523,057 B1 2/2003 Savo et al. 7,865,541 B1 1/2011 Langhammer (6,531,888 B2 3/2003 Abbott 7,917,567 B1 3/2011 Mason et al. (6,538,470 B1 3/2003 Langhammer et al. 7,930,335 B2 4/2011 Gura (6,542,000 B1 4/2003 Black et al. 7,930,336 B2 4/2011 Langhammer (6,556,044 B2 4/2003 Langhammer et al. 7,949,699 B1 5/2011 Neoh et al. (6,557,092 B1 4/2003 Callen 7,974,997 B2 7/2011 Arviv et al. (6,573,749 B2 6/2003 New et al. 8,041,759 B1 10/2011 Langhammer et al. (6,573,749 B2 6/2003 Karimi et al. 8,112,466 B2 2/2012 Minz et al.					
6,487,575 B1 11/2002 Oberman 7,822,799 B1 10/2010 Langhammer et al. 6,523,055 B1 2/2003 Yu et al. 7,836,117 B1 11/2010 Langhammer et al. 6,523,057 B1 2/2003 Savo et al. 7,865,541 B1 1/2011 Langhammer 6,531,888 B2 3/2003 Abbott 7,917,567 B1 3/2011 Mason et al. 6,538,470 B1 3/2003 Langhammer et al. 7,930,335 B2 4/2011 Gura 6,542,000 B1 4/2003 Black et al. 7,930,336 B2 4/2011 Langhammer 6,556,044 B2 4/2003 Langhammer et al. 7,949,699 B1 5/2011 Neoh et al. 6,557,092 B1 4/2003 Callen 7,974,997 B2 7/2011 Arviv et al. 6,571,268 B1 5/2003 Giacalone et al. 8,041,759 B1 10/2011 Langhammer et al. 6,573,749 B2 6/2003 New et al. 8,090,758 B1 1/2012 Shimanek et al. 6,574,762 B1 6/2003 Karimi et al. 8,112,466 B2 2/2012 Minz et al.					
6,523,055 B1					
6,523,057 B1       2/2003 Savo et al.       7,865,541 B1       1/2011 Langhammer         6,531,888 B2       3/2003 Abbott       7,917,567 B1       3/2011 Mason et al.         6,538,470 B1       3/2003 Langhammer et al.       7,930,335 B2       4/2011 Gura         6,542,000 B1       4/2003 Black et al.       7,930,336 B2       4/2011 Langhammer         6,556,044 B2       4/2003 Langhammer et al.       7,949,699 B1       5/2011 Neoh et al.         6,557,092 B1       4/2003 Callen       7,974,997 B2       7/2011 Arviv et al.         6,571,268 B1       5/2003 Giacalone et al.       8,041,759 B1       10/2011 Langhammer et al.         6,573,749 B2       6/2003 New et al.       8,090,758 B1       1/2012 Shimanek et al.         6,574,762 B1       6/2003 Karimi et al.       8,112,466 B2       2/2012 Minz et al.			7,836,117 B1	11/2010	Langhammer et al.
6,538,470 B1 3/2003 Langhammer et al. 7,930,335 B2 4/2011 Gura 6,542,000 B1 4/2003 Black et al. 7,930,336 B2 4/2011 Langhammer 6,556,044 B2 4/2003 Langhammer et al. 7,949,699 B1 5/2011 Neoh et al. 6,557,092 B1 4/2003 Callen 7,974,997 B2 7/2011 Arviv et al. 6,571,268 B1 5/2003 Giacalone et al. 8,041,759 B1 10/2011 Langhammer et al. 6,573,749 B2 6/2003 New et al. 8,090,758 B1 1/2012 Shimanek et al. 6,574,762 B1 6/2003 Karimi et al. 8,112,466 B2 2/2012 Minz et al.	6,523,057 B1 2/2003	Savo et al.			~
6,542,000 B1       4/2003 Black et al.       7,930,336 B2       4/2011 Langhammer         6,556,044 B2       4/2003 Langhammer et al.       7,949,699 B1       5/2011 Neoh et al.         6,557,092 B1       4/2003 Callen       7,974,997 B2       7/2011 Arviv et al.         6,571,268 B1       5/2003 Giacalone et al.       8,041,759 B1       10/2011 Langhammer et al.         6,573,749 B2       6/2003 New et al.       8,090,758 B1       1/2012 Shimanek et al.         6,574,762 B1       6/2003 Karimi et al.       8,112,466 B2       2/2012 Minz et al.					
6,556,044 B2       4/2003 Langhammer et al.       7,949,699 B1       5/2011 Neoh et al.         6,557,092 B1       4/2003 Callen       7,974,997 B2       7/2011 Arviv et al.         6,571,268 B1       5/2003 Giacalone et al.       8,041,759 B1       10/2011 Langhammer et al.         6,573,749 B2       6/2003 New et al.       8,090,758 B1       1/2012 Shimanek et al.         6,574,762 B1       6/2003 Karimi et al.       8,112,466 B2       2/2012 Minz et al.					
6,571,268 B1       5/2003 Giacalone et al.       8,041,759 B1       10/2011 Langhammer et al.         6,573,749 B2       6/2003 New et al.       8,090,758 B1       1/2012 Shimanek et al.         6,574,762 B1       6/2003 Karimi et al.       8,112,466 B2       2/2012 Minz et al.			7,949,699 B1		
6,573,749 B2 6/2003 New et al. 8,090,758 B1 1/2012 Shimanek et al. 6,574,762 B1 6/2003 Karimi et al. 8,112,466 B2 2/2012 Minz et al.					
6,574,762 B1 6/2003 Karimi et al. 8,112,466 B2 2/2012 Minz et al.					

S. PATENT DOCUMENTS	(56)	Referen	ces Cited		FOREIGN PAT	TENT DOCUMEN	TS
B	U.S.	PATENT	DOCUMENTS	EP	0 380 456	8/1990	
8,386,550 Bl 2,2013 Maser et al. FP 0,461 798 [21]991 8,386,553 Bl 2,2013 Langhammer et al. FP 0,498 866 81]992 8,396,914 Bl 3,2013 Langhammer et al. FP 0,498 866 81]992 8,396,914 Bl 3,2013 Langhammer et al. FP 0,555 902 81]903 8,386,553 Al 9,2001 Oberman et al. FP 0,555 902 81]903 8,001,002,002,002,002,002,002,002,002,002	0.2.						
8.386,553 Bi	8,307,023 B1	11/2012	Leung et al.		0 419 105	3/1991	
8,396,914 Bl 3 2013 Langhammer EP 0,555 092 8,1993 (2010/02348) 4 92001 Oberman et al. EP 0,666 653 7,1994 (2010/02378) 41 112001 Hong EP 0,667 803 6,1995 (2010/02378) 41 112001 Hong EP 0,677 803 6,1995 (2010/02378) 41 112001 Hong EP 0,678 803 6,1995 (2010/02378) 41 112001 Hong EP 0,678 803 6,1995 (2010/02378) 41 112001 Hong EP 0,678 803 6,1995 (2010/02378) 41 112001 Hong EP 0,971 159 8,1995 (2010/02378) 41 112002 Hong et al. EP 0,990 208 41,1999 (2010/02378) 41 112002 Hong et al. EP 0,972 803 7,1996 (2010/02378) 41 112002 (2010/02378) 41 72002 (2010/02378) 41 72002 (2010/02378) 41 72002 (2010/02378) 41 72002 (2010/02378) 41 72002 (2010/02378) 41 72002 (2010/02378) 41 72002 (2010/02378) 41 72003 (2010/02378) 41 72004 (2010/02378) 41 72004 (2010/02378) 41 72004 (2010/02378) 41 72004 (2010/02378) 41 72004 (2010/0388) 41 7	8,386,550 B1	2/2013	Mauer et al.				
Dept.   Dept	, ,						
1.001003915   Al   10.2001   Minsky   EP   0.657 803   61995	, ,						
120010037351   A1   11/2001   Hellbery   EP   0 660 227   61/995							
12001093745   Al   11/2001   Hong   EP   0 688 659   81/995							
2002/0003873 Al   1,2002   Landers et al.							
2002-0032713 A1 3/2002   Joue et al.   FP							
2002/00/38124							
2002/0094798							
2002/0078114 A1 6/2002   Wang et al.   EP	2002/0049798 A1						
2002.0116434   A1   8.2002   Nacekievill   EP   1.05s 185   12.2000   2003.0008757   A1   5.2003   Lindure et al.   GB   2.285 602   5.1995   2004.000877   A1   4.2004   Xin   GB   2.286 73   5.1995   2004.00083412   A1   4.2004   Corbin et al.   GB   2.285 602   5.1995   2004.00083412   A1   4.2004   Corbin et al.   GB   2.286 73   5.1995   2004.00083412   A1   4.2004   Corbin et al.   GB   2.286 73   5.1995   2004.00163331   A1   5.2004   Commerce of al.   PR   6.321613   GB   Corbinal of al.   PR   6.321613   GB	2002/0078114 A1						
2002/0129073 Al   9,2002   Page et al.   EP   1,200 108   7,2002					1 049 025	11/2000	
2004/006734							
2004/006470, Al.   4/2004   Xim.   GB   2/38/6737   8/1995							
2004-0033142 Al							
2004-0103133   Al   5/2004   Gurney   JP   61-237133   10/1986							
2004/01   22882   Al   6'2004   Zakharov et al   JP   63-2   631  8   8   8   2004/01   231   Al   7'2004   Guevorkian et al   JP   5-134851   6   6   903     2004/01   249   Al   9'2004   Guevorkian et al   JP   5-134851   6   6   903     2004/01   249   Al   9'2004   Corty et al   JP   6-187129   7   994     2004/01   27873   Al   12'2004   Corty et al   JP   7-135447   5   995     2004/0128783   Al   12'2004   Bhushan et al   JP   2000-259394   9   9   9   9   9   9   9   9   9							
2004/0148321 Al						8/1988	
Display							
2004/01/8818 Al   9.2004   Clark et al.   JP   7-135447   5/1995   2004/0267857 Al   12/2004   Clark et al.   JP   11-296445   10/1999   2005/026363 Al   12/2004   Blushan et al.   JP   2000-259394   9/2000   2005/03038842   Al   2/2005   Sarkhan et al.   JP   2002-251281   9/2002   2005/031212 Al   6/2005   Farnham   WO   WO95/27743   9/1996   2005/03144215   Al   6/2005   Simkins et al.   WO   WO96/28774   9/1996   2005/03144216   Al   6/2005   Simkins et al.   WO   WO98/3774   9/1996   2005/03144216   Al   6/2005   Simkins et al.   WO   WO98/3774   9/1996   2005/03144216   Al   6/2005   Simkins et al.   WO   WO98/3774   9/1996   2005/03144216   Al   6/2005   Simkins et al.   WO   WO98/3774   9/1998   2005/03187997   Al   8/2005   Wang et al.   WO   WO98/38741   9/1998   2005/0362175   Al   11/2005   Zibeng et al.   WO   WO99/31574   6/1999   2005/0262175   Al   11/2005   Zibeng et al.   WO   WO99/31574   6/1999   2006/00205215   Al   2/2006   Sibhi et al.   WO   WO99/31574   6/1999   2006/0020722   Al   2/2006   Sibhi et al.   WO   WO99/31574   6/1999   2006/0020723   Al   2/2006   Sibhi et al.   WO   WO99/31574   6/1999   2006/0020723   Al   2/2006   Sibhi et al.   WO   WO99/31574   6/1999   2006/0020723   Al   2/2006   Sibhi et al.   WO   WO99/31574   6/1999   2006/0020723   Al   2/2006   Sibhi et al.   WO   WO99/31574   6/1999   2006/0020723   Al   2/2006   Sibhi et al.   WO   WO99/31574   6/1999   2006/0020723   Al   2/2006   Sibhi et al.   WO   WO99/31574   6/1999   2/2006/0020723   Al   2/2006   Sibhi et al.   WO   WO99/31574   6/1999   2/2006/0020723   Al   2/2006   Sibhi et al.   WO   WO99/31574   6/1999   2/2006/0020723   Al   2/2006   Sibhi et al.   WO   WO99/31574   6/1999   2/2006/0020723   Al   2/2006   Sibhi et al.   WO   WO99/31574   6/1999   2/2006/0020723   Al   2/2006   Sibhi et al.   WO   WO99/31574   6/1999   Al   2/2006   Sibhi et al.   WO   WO99/31574   6/1999   Al   2/2006   Sibhi et al.   WO   WO99/31574   6/1999   Al   2/2007   Al   2/2007   Al   2/2007   Al   2/2007   Al   2/2007		9/2004	Lin				
2004/01/267863   Al   2/2004   Abel et al.   JP   11-296345   10/1999   2004/02/67863   Al   12/2004   Abel et al.   JP   2002-253894   9/2000   2005/03/8842   Al   2/2005   Stoye   JP   2002-251281   9/2002   2005/03/8421   Al   6/2005   Simkins et al.   WO   WO95/27/243   10/1995   2005/03/4212   Al   6/2005   Simkins et al.   WO   WO95/27/243   10/1995   2005/03/4215   Al   6/2005   Simkins et al.   WO   WO95/27/243   10/1995   2005/03/14215   Al   6/2005   Simkins et al.   WO   WO95/27/243   10/1995   2005/03/14215   Al   6/2005   Simkins et al.   WO   WO97/08/606   3/1997   Al   2005/03/14215   Al   6/2005   Simkins et al.   WO   WO98/32071   7/1998   Al   2005/03/187997   Al   8/2005   Zheng et al.   WO   WO98/32071   7/1998   Al   2005/03/187999   Al   8/2005   Zheng et al.   WO   WO99/32071   7/1998   Al   2005/03/187999   Al   8/2005   Zheng et al.   WO   WO99/32071   7/1998   Al   2005/03/187999   Al   8/2005   Zheng et al.   WO   WO99/32071   7/1998   Al   2005/03/187999   Al   8/2005   Zheng et al.   WO   WO99/32071   7/1998   Al   2005/03/187999   Al   8/2005   Zheng et al.   WO   WO99/32071   7/1998   Al   2005/05/05/05/1999   Al   2005/05/05/1999   Al   2005/05/05/	2004/0178818 A1	9/2004	Crotty et al.				
2004/02/67867 A 1 12/2004 2005/0303842 A1 2/2005 2005/0303842 A1 2/2005 2005/0303842 A1 2/2005 2005/0303842 A1 2/2005 2005/0304212 A1 6/2005 2005/0304216 A1 6/2005 2005/0304216 A1 6/2005 2005/0304216 A1 6/2005 2005/030420 A1 7/2005 200							
2005/0013842   Al   22005   Stoye   1P   2002-25188   9/2002   2005/0014212   Al   6/2005   Simkins et al.   WO   WO95/27243   10/1995   WO 9/005/00144215   Al   6/2005   Simkins et al.   WO   WO96/28774   9/1996   WO95/005/0144215   Al   6/2005   Simkins et al.   WO   WO97/08066   3/1997   2005/0144215   Al   6/2005   Simkins et al.   WO   WO98/18229   3/1998   WO 9/005/0144215   Al   6/2005   Simkins et al.   WO   WO98/182207   7/1998   2005/0166038   Al   7/2005   Wang et al.   WO   WO98/38741   9/1998   2005/0167997   Al   8/2005   Zheng et al.   WO   WO98/3874   6/1999   2005/016737   Al   1/2005   In   WO   WO99/31574   6/1999   2005/026715   Al   1/2005   In   WO   WO99/31574   6/1999   2006/0059215   Al   3/2006   Maharatna et al.   WO   WO99/31574   6/1999   2/2006/0059215   Al   3/2006   Maharatna et al.   WO   WO99/31574   6/1999   2/2006/0059215   Al   3/2006   Maharatna et al.   WO   WO09/31574   6/1999   2/2006/0059215   Al   3/2006   Maharatna et al.   WO   WO09/31574   6/1999   2/2006/0059215   Al   3/2006   Maharatna et al.   WO   WO09/31574   6/1999   2/2006/0059215   Al   3/2007   Maharatna et al.   WO   WO09/31574   6/1999   2/2006/0059215   Al   3/2007   Wittig   WO   WO09/31574   6/1999   2/2006/0059215   Al   3/2007   Wittig   WO   WO   2/2005/0058338   Al   4/2007   St. Denis et al.   WO   WO   2/2005/0058338   Al   4/2007   St. Denis et al.   WO   WO   2/2005/0058338   Al   4/2007   Wittig   WO   WO   2/2005/0058338   Al   4/2007   Woode   Alexandra et al.   WO   WO   2/2005/0058338   Al   4/2007   Woode   Alexandra et al.   WO   WO   2/2005/0058338   Al   4/2007   Woode   Alexandra et al.   WO   WO   2/2005/0058338   Al   4/2007   Woode   Alexandra et al.   WO   WO   2/2005/0058338   Al   4/2007   Woode   Alexandra et al.   WO   WO   2/2005/0058338   Al   4/2007   Woode   Alexandra et al.   WO   WO   2/2005/0058338   Al   4/2007   Woode   Alexandra et al.   Woode   Alexandra et							
2005/014212 Al 6/2005   Simkins et al.   WO W095/27243   10/1996					2002-108606	4/2002	
2005/0144215 Al 6/2005 Simkins et al.   WO   WO96/28774   9/1996							
2005/0144216 Al 6/2005 Simkins et al.   WO WO98/12629 3/1998							
2005/0144216 A1							
2005/0166038 Al   7/2005   Xeng et al.   WO   WO98/32071   7/1998   2005/0187997   Al   8/2005   Zheng et al.   WO   WO99/32292   5/1999   2005/0187999   Al   8/2005   Zheng et al.   WO   WO99/31574   6/1999   2005/0262175   Al   11/2006   Lino et al.   WO   WO99/31574   6/1999   2006/0200655   Al   1/2006   Lino et al.   WO   WO99/32894   11/1999   2006/0200655   Al   3/2006   Maharatna et al.   WO   WO99/3284   9/2000   2006/0200732   Al   9/2006   Dobbek et al.   WO   WO00/51239   8/2000   2007/024352   Al   9/2006   Dobbek et al.   WO   WO00/52824   9/2000   2007/024352   Al   2/2007   Uritig   WO   WO 2005/06832   7/2005   2007/0183595   Al   8/2007   Lee et al.   WO   WO 2005/06832   7/2005   2007/0185951   Al   8/2007   Lee et al.   WO   WO 2005/010190   10/2005   2007/0241773   Al   10/2007   Hutchings et al.   WO   WO 2005/03637   Al   2/2007   Lin et al.   WO   WO 2005/03637   Al   2/2007   Lin et al.   WO   WO 2005/03637   Al   2/2008   Liao et al.   Altera Corporation, "Stratix II Device Handbook, Chapter 6—DSP 2008/013367   Al   7/2008   Liao et al.   Altera Corporation, "Digital Signal Processing (DSP)," Stratix 2009/0028455   Al   1/2009   Nakamura et al.   Altera Corporation, "Dispital Signal Processing (DSP)," Stratix 2009/012352   Al   7/2009   Alen   Devices Handbook, vol. 2, Chapter 6, v4.0 (Oct. 2005)   Altera Corporation, "Dispital Signal Processing (DSP)," Stratix 1009/013186   Al   4/2009   Al   2/2009   Al							
2005/0187997 Al   8/2005   Zheng et al.   WO   WO98/38741   9/1998   2005/0262175   Al   11/2005   Ino et al.   WO   WO99/31574   6/1999   2005/0262175   Al   11/2005   Ino et al.   WO   WO99/31574   6/1999   2006/0020655   Al   2006   2006/0202051   Al   3/2006   Maharatna et al.   WO   WO99/31534   6/1999   8/2000   2006/02020721   Al   3/2006   Shiri et al.   WO   WO00/51239   8/2000   WO00/030232   Al   9/2000   Dobbek et al.   WO   WO00/51239   8/2000   WO00/030232   Al   9/2000   Dobbek et al.   WO   WO01/31562   2/2001   2007/018355   Al   4/2007   St. Denis et al.   WO   WO 2005/066832   7/2005   2007/0124352   Al   5/2007   Wittig   WO   WO 2005/011190   10/2005   2007/0185951   Al   8/2007   Lee et al.   WO   WO 2005/011190   10/2005   2007/0185951   Al   8/2007   Lee et al.   WO   WO 2005/01190   10/2005   2007/0185951   Al   8/2007   Lee et al.   WO   WO 2005/01190   10/2005   2007/0185951   Al   8/2007   Lee et al.   WO   WO 2005/01190   10/2005   2007/0185951   Al   8/2007   Lee et al.   WO   WO 2005/01190   10/2005   2007/0185951   Al   8/2007   Lee et al.   WO   WO 2005/01190   10/2005   2007/0185951   Al   4/2008   Al   4/2008   Al   4/2008   Al   4/2008   Al   4/2009   Al   4/2010				WO			
2005/0262175 A1         11/2005         Lin         WO         WO99/36394         11/1999           2006/0020655 A1         1/2006         Lin         WO         WO99/56394         11/1999           2006/0059215 A1         3/2006         Ishii et al.         WO         WO00/51239         8/2000           2006/0020732 A1         9/2006         Dobbek et al.         WO         WO01/13562         2/2001           2007/0083585 A1         4/2007         Wittig         WO         WO 2005/066832         7/2005           2007/0124352 A1         5/2007         Wittig         WO         WO 2005/10190         10/2005           2007/0185952 A1         8/2007         Lae et al.         WO         WO 2010/102007         9/2010           2007/0226287 A1         9/2007         Hutchings et al.         Altera Corporation, "Stratix II Device Handbook, Chapter 6—DSP           2008/0133627 A1         6/2008         Langhammer et al.         Blocks in Stratix II Device Handbook, Chapter 6—DSP           2008/015841 A1         7/2008         Liac et al.         Blocks in Stratix II and Stratix II Gas et al.           2008/013378 A1         1/2009         Nakamura et al.         Altera Corporation, "DSP Blocks in Stratix II and Stratix II Gas et al.           2009/013158 A1         1/2009         Na	2005/0187997 A1	8/2005	Zheng et al.				
2006/0020655 A1   1/2006   Lin   WO   WO09/56394   11/1999   2006/012160   A1   3/2006   Maharatna et al.   WO   WO00/51239   8/2000   2006/012160   A1   3/2006   Maharatna et al.   WO   WO00/51239   8/2000   2006/0200732   A1   9/2006   Dobbek et al.   WO   WO01/13562   2/2001   2007/0083585   A1   4/2007   St. Denis et al.   WO   WO 2005/101190   10/2005   2007/0124352   A1   5/2007   Lee et al.   WO   WO 2005/101190   10/2005   2007/0185951   A1   8/2007   Lee et al.   WO   WO 2005/101190   10/2005   2007/0185952   A1   8/2007   Langhammer et al.   WO   WO 2010/102007   9/2010   2007/0185952   A1   8/2007   Langhammer et al.   WO   WO 2010/102007   9/2010   2007/0183627   A1   0/2007   Lin et al.   Altera Corporation, "Stratix II Device Handbook, Chapter 6—DSP   2008/0133627   A1   6/2008   Langhammer et al.   Blocks in Stratix II Devices;" V1-1, Jul. 2004.   Altera Corporation, "Digital Signal Processing (DSP)," Stratix 2008/0183783   A1   7/2008   Liao et al.   Altera Corporation, "Digital Signal Processing (DSP)," Stratix Union of the process of t	2005/0187999 A1						
WO   WO00/51239   8,2000							
WO   WO0052824   9/2000							
2006/0200732 Al   9/2006   Dobbek et al.   WO   WO01/13562   2/2001							
2007/083585 Al   4/2007 St. Denis et al.   WO   WO 2005/101190   10/2005   10/2005   2007/0124352   Al   5/2007   Wittig   WO   WO 2010/102007   9/2010   2007/0185951   Al   8/2007   Lee et al.   WO   WO 2010/102007   9/2010   2007/0185952   Al   8/2007   Lee et al.   WO   WO 2010/102007   9/2010   2007/0226287   Al   9/2007   Lin et al.   Altera Corporation, "Stratix II Device Handbook, Chapter 6—DSP   2008/0133627   Al   6/2008   Langhammer et al.   Blocks in Stratix II Devices," v1.1, Jul. 2004.   Altera Corporation, "Digital Signal Processing (DSP)," Stratix 2008/0183783   Al   7/2008   Liao et al.   Altera Corporation, "Digital Signal Processing (DSP)," Stratix 2008/0183783   Al   7/2008   Liao et al.   Altera Corporation, "Digital Signal Processing (DSP)," Stratix 1209/0028455   Al   1/2009   Altera Corporation, "Digital Signal Processing (DSP)," Stratix 1209/0028455   Al   1/2009   Altera Corporation, "Digital Device Handbook, vol. 2, Chapter 6, v4.0 (Oct. 2009/0113186   Al   4/2009   Kato et al.   2009/0113186   Al   4/2009   Kato et al.   2009/0127052   Al   7/2009   DeLaquil et al.   2009/0137615   Al   7/2009   DeLaquil et al.   2009/0300088   Al   2/2009   Michaels et al.   4/2009   Kato et al.   2009/0300088   Al   2/2009   Michaels et al.   2/2009   Mich					WO01/13562		
2007/0124352 A1 5/2007 Wittig WO WO 2010/102007 9/2010 2007/0185951 A1 8/2007 Lee et al. 2007/0226287 A1 9/2007 Lin et al. 2007/0241773 A1 10/2007 Hutchings et al. 2007/0241773 A1 10/2007 Hutchings et al. 2008/0159441 A1 7/2008 Liao et al. 2008/0183783 A1 7/2008 Tubbs Device-Handbook, vol. 2, Chapter 6 and Chapter 7, v1. 1 (Sep. 2004). 2009/0028455 A1 1/2009 Nakamura et al. 2009/0028455 A1 3/2009 Allen Devices," Stratix II Device Handbook, vol. 2, Chapter 6 and Chapter 7, v1. 1 (Sep. 2004). 2009/013186 A1 4/2009 Kato et al. 2009/013205 A1 7/2009 DeLaquil et al. 2009/01252 A1 7/2009 Muff et al. 2009/0300088 A1 1/2/2009 Michaels et al. 2010/0098189 A1 4/2010 Oketani 2010/0131577 A1 5/2010 Gangalakurti et al. 2010/0146022 A1 6/2010 Swartzlander et al. 2010/0146022 A1 6/2010 Swartzlander et al. 2011/0238720 A1 9/2011 Langhammer 2011/0328720 A1 3/2012 Langhammer et al. 2011/0328720 A1 3/2012 Langhammer et al. 2012/0054256 A1 3/2012 Langhammer 2012/0156512 A1 7/2012 Langhammer 2012/0156133 A1 5/2012 Spipigelblat A 7/2012 Lin et al. 2012/0156151 A1 7/2009 Midf et al. 2012/0156151 A1 7/2009 Muff et al. 2011/0328720 A1 9/2011 Langhammer 2011/0328720 A1 9/2011 Langhammer 2011/031333 A1 5/2012 Langhammer 2012/0156152 A1 3/2012 Langhammer 2012/0156152 A1 3/2012 Langhammer 2012/0156152 A1 3/2012 Langhammer 2012/0156154 A1 3/2012 Langhammer 2012/0156151 A1 7/2012 Wong et al. 2012/0156151 A1 7/2012 Lin et al. 2012/0156151 A1							
2007/0185951   Al   8/2007   Lee et al.   2007/01859552   Al   8/2007   Langhammer et al.   2007/0226287   Al   9/2007   Lin et al.   2007/0226287   Al   9/2007   Lin et al.   2007/0226287   Al   9/2007   Lin et al.   2007/0226287   Al   10/2007   Hutchings et al.   2007/0241773   Al   10/2007   Hutchings et al.   2008/0133627   Al   6/2008   Langhammer et al.   2008/0159441   Al   7/2008   Liao et al.   Altera Corporation, "Stratix II Device," vl.1, Jul. 2004.   Altera Corporation, "Orgital Signal Processing (DSP)," Stratix 2008/0183783   Al   7/2008   Tubbs   Device Handbook, vol. 2, Chapter 6 and Chapter 7, vl.1 (Sep. 2004).   Altera Corporation, "DSP Blocks in Stratix II and Stratix II GX 2009/033358   Al   3/2009   Altera   Altera Corporation, "DSP Blocks in Stratix II and Stratix II GX 2009/0172052   Al   2/2009   Kato et al.   2005.   Altera Corporation, "FIR Compiler: MegaCore® Function User 2009/0187615   Al   7/2009   Del. aquil et al.   Altera Corporation, "FIR Compiler: MegaCore® Function User 2009/028689   Al   9/2009   Muff et al.   Guide," version 3.3.0, rev. 1, pp. 3 11 through 3 15 (Oct. 2005).   Altera Corporation, "Advanced Synthesis Cookbook: A Design 2010/0398189   Al   4/2010   Oketani   Altera Corporation, "Advanced Synthesis Cookbook: A Design 2010/0181577   Al   5/2010   Gangalakurti et al.   Guide for Stratix II, Stratix III and Stratix IV Devices," Document 2011/02138720   Al   9/2011   Langhammer et al.   2011/02138720   Al   9/2011   Langhammer et al.   2011/03238720   Al   9/2011   Langhammer   2012/0054254   Al   3/2012   Langhammer   2012/0054256   Al   3/2012   Langhammer   2012/0054256   Al   3/2012   Lan							
2007/0226287 A1 9/2007 Lin et al. 2007/0241773 A1 10/2007 Hutchings et al. 2008/0133627 A1 6/2008 Langhammer et al. 2008/0159441 A1 7/2008 Liao et al. 2008/0159441 A1 7/2008 Liao et al. 2008/0183783 A1 7/2008 Tubbs Device Handbook, vol. 2, Chapter 6 and Chapter 7, v1.1 (Sep. 2004). 2009/0028455 A1 1/2009 Nakamura et al. 2009/0013186 A1 4/2009 Kato et al. 2009/0113186 A1 4/2009 Kato et al. 2009/0172052 A1 7/2009 DeLaquil et al. 2009/0128689 A1 9/2009 Muff et al. 2010/0038189 A1 4/2010 Oketani 2010/0131577 A1 5/2010 Gangalakurti et al. 2010/0131939 A1 7/2010 Muff et al. 2010/0191939 A1 7/2010 Muff et al. 2011/0238720 A1 9/2011 Langhammer et al. 2011/0238720 A1 9/2011 Langhammer et al. 2011/0238720 A1 9/2011 Langhammer et al. 2011/0320513 A1 1/2/2011 Langhammer et al. 2012/0054254 A1 3/2012 Langhammer et al. 2012/0156512 A1 6/2012 Wong et al. 2012/0166512 A1 6/2012 Wong et al. 2012/0191967 A1 7/2012 Lin et al.  Altera Corporation, "Stratix II Device Handbook, Chapter 6—DSP Blocks in Stratix II Devices," v1.1, Jul. 2004. Altera Corporation, "Digital Signal Processing (DSP)," Stratix II GX Devices, "Stratix II Device Handbook, Chapter 6—DSP Blocks in Stratix II Devices," v1.1, Jul. 2004. Altera Corporation, "Digital Signal Processing (DSP)," Stratix II GX Devices, "Stratix II Device Handbook, vol. 2, Chapter 6—DSP Altera Corporation, "DSP Blocks in Stratix II and Stratix II GX Devices," Stratix II Device Handbook, vol. 2, Chapter 6—DSP Delaqued Corporation, "Digital Signal Processing (DSP)," Stratix II GX Devices, "Stratix II Device Handbook, vol. 2, Chapter 6—DSP Altera Corporation, "Digital Signal Processing (DSP)," Stratix II GX Devices," Stratix II Device Handbook, vol. 2, Chapter 6, v4.0 (Oct. 2005). Altera Corporation, "Stratix II Device Handbook, vol. 2, Chapter 6, v4.0 (Oct. 2005). Altera Corporation, "BIR Compiler: MegaCore® Function User Guide for Stratix II, Stratix II stratix II and Stratix II Vol. (Sci. 2005). Altera Corporation, "Stratix II, Stratix II and Stratix IV Devices," Decument Version 3.0, rev				wo	WO 2010/102007	9/2010	
2007/0241773 A1 10/2007 Hutchings et al. 2008/0133627 A1 6/2008 Langhammer et al. 2008/0133627 A1 6/2008 Liao et al. 2008/0159441 A1 7/2008 Liao et al. 2008/0159441 A1 7/2008 Tubbs Blocks in Stratix II Devices, "V1.1, Jul. 2004. Altera Corporation, "Digital Signal Processing (DSP)," Stratix 2008/0183783 A1 7/2008 Tubbs Device Handbook, vol. 2, Chapter 6 and Chapter 7, v1.1 (Sep. 2004). Altera Corporation, "Digital Signal Processing (DSP)," Stratix 2008/0083358 A1 3/2009 Allen Devices," Stratix II Device Handbook, vol. 2, Chapter 6, v4.0 (Oct. 2009/013186 A1 4/2009 Kato et al. 2009/0172052 A1 7/2009 DeLaquil et al. 2009/0172052 A1 7/2009 DeLaquil et al. 2009/0187615 A1 7/2009 Abe et al. 2009/0300088 A1 2009/0300088 A1 2009/0300088 A1 2009/0300088 A1 2/2009 Muff et al. 2009/0300088 A1 2/2009 Michaels et al. 2010/00146022 A1 2010/0191939 A1 4/2010 Oketani 2010/0191939 A1 7/2010 Muff et al. 2010/0146022 A1 6/2010 Savatzlander et al. 2010/0146022 A1 6/2010 Muff et al. 2011/0238720 A1 9/2011 Langhammer et al. 2011/0238720 A1 9/2011 Langhammer et al. 2011/0320513 A1 12/2011 Langhammer et al. 2011/0320513 A1 12/2011 Langhammer et al. 2012/0054254 A1 3/2012 Langhammer 41 2012/0054254 A1	2007/0185952 A1				OTHER F	PUBLICATIONS	
2008/0133627 A1 6/2008 Langhammer et al. 2008/0159441 A1 7/2008 Liao et al. Altera Corporation, "Digital Signal Processing (DSP)," Stratix 2008/0183783 A1 7/2008 Tubbs Device Handbook, vol. 2, Chapter 6 and Chapter 7, v1.1 (Sep. 2004). Altera Corporation, "DSP Blocks in Stratix II and Stratix II GX 2009/0028455 A1 1/2009 Nakamura et al. Altera Corporation, "DSP Blocks in Stratix II and Stratix II GX 2009/0113186 A1 4/2009 Kato et al. 2005). 2009/0172052 A1 7/2009 DeLaquil et al. 2005/0187615 A1 7/2009 Abe et al. Altera Corporation, "FIR Compiler: MegaCore® Function User 2009/0187615 A1 7/2009 Abe et al. 4/2010 Michaels et al. 2005/0300088 A1 1/2/2009 Michaels et al. 2009/0300088 A1 1/2/2009 Michaels et al. 2010/0098189 A1 4/2010 Oketani 2010/0131577 A1 5/2010 Gangalakurti et al. 2010/0146022 A1 6/2010 Swartzlander et al. 2010/0191939 A1 7/2010 Muff et al. 2010/0131573 A1 2010/0131537 A1 2010/013153 A1 1/2/2011 Langhammer et al. 2011/0238720 A1 9/2011 Langhammer et al. 2011/0328720 A1 9/2011 Langhammer et al. 2011/0328720 A1 9/2011 Langhammer et al. 2011/0328720 A1 1/2/2011 Langhammer et al. 2011/0328720 A1 1/2/2011 Langhammer et al. 2011/0328720 A1 3/2012 Langhammer 2011/0328720 A1 3/2012 Shpigelblat 2012/0054254 A1 3/2012 Shpigelblat 456-461. 2012/0191967 A1 5/2012 Using et al. 40ki, T., "Signed-weight arithmetic and its application to a field-programmable digital filter architecture," IEICE Transactions on							
2008/0159441 A1 7/2008 Liao et al. Altera Corporation, "Digital Signal Processing (DSP)," Stratix 2008/0183783 A1 7/2008 Tubbs Device Handbook, vol. 2, Chapter 6 and Chapter 7, vl.1 (Sep. 2004). Altera Corporation, "DSP Blocks in Stratix II and Stratix II and Stratix II and Stratix II Devices," Stratix II Devices, II De							Chapter 6—DSP
2008/0183783 A1 7/2008 Tubbs 2009/0028455 A1 1/2009 Nakamura et al. 2009/0183358 A1 3/2009 Allen 2009/0113186 A1 4/2009 Kato et al. 2009/0172052 A1 7/2009 DeLaquil et al. 2009/0187615 A1 7/2009 Muff et al. 2009/0308088 A1 12/2009 Muff et al. 2010/0131577 A1 5/2010 Gangalakurti et al. 2010/0146022 A1 6/2010 Swartzlander et al. 2010/0191939 A1 7/2010 Muff et al. 2010/0191935 A1 7/2010 Muff et al. 2010/0238720 A1 9/2011 Langhammer et al. 2011/0238720 A1 3/2012 Langhammer et al. 2011/0038721 A1 1/2011 Langhammer et al. 2011/0038720 A1 3/2012 Langhammer et al. 2012/0054256 A1 3/2012 Langhammer et al. 2012/0113133 A1 5/2012 Shpigelblat 2012/0113133 A1 5/2012 Shpigelblat 2012/01191967 A1 7/2012 Lin et al. 2012/0191967 A1 7/2012 Lin et al. 2018/2009 Nakamura et al. 20205). Altera Corporation, "FIR Compiler: MegaCore® Function User Guide," version 3.3.0, rev. 1, pp. 3 11 through 3 15 (Oct. 2005). Altera Corporation, "FIR Compiler: MegaCore® Function User Guide," version 3.3.0, rev. 1, pp. 3 11 through 3 15 (Oct. 2005). Altera Corporation, "FIR Compiler: MegaCore® Function User Guide," version 3.3.0, rev. 1, pp. 3 11 through 3 15 (Oct. 2005). Altera Corporation, "FIR Compiler: MegaCore® Function User Guide," version 3.3.0, rev. 1, pp. 3 11 through 3 15 (Oct. 2005). Altera Corporation, "FIR Compiler: MegaCore® Function User Guide," version 3.3.0, rev. 1, pp. 3 11 through 3 15 (Oct. 2005). Altera Corporation, "FIR Compiler: MegaCore® Function User Guide," version 3.3.0, rev. 1, pp. 3 11 through 3 15 (Oct. 2005). Altera Corporation, "FIR Compiler: MegaCore® Function User Guide," version 3.3.0, rev. 1, pp. 3 11 through 3 15 (Oct. 2005). Altera Corporation, "FIR Compiler: MegaCore® Aller Corporation on "Advanced Synthesis Cookbook. A Design Guide," version 3.3.0, rev. 1, pp. 3 11 through 3 15 (Oct. 2005). Altera Corporation,							(DCD) ? C44i
2009/0028455 A1 1/2009 Nakamura et al. 2009/0083358 A1 3/2009 Allen 2009/01872052 A1 7/2009 DeLaquil et al. 2009/0187615 A1 7/2009 Abe et al. 2009/0228689 A1 9/2009 Muff et al. 2010/0098189 A1 4/2010 Oketani 2010/0131577 A1 5/2010 Gangalakurti et al. 2010/0191939 A1 7/2010 Muff et al. 2010/0191939 A1 7/2010 Muff et al. 2010/0191935 A1 6/2011 Langhammer et al. 2011/0238720 A1 9/2011 Langhammer 2011/0320513 A1 12/2011 Langhammer 2012/0054254 A1 3/2012 Langhammer 2012/0166512 A1 6/2012 Wong et al. 2012/0191967 A1 7/2012 Lin et al. 2012/0191967 A1 7/2012 Lin et al.  Altera Corporation, "EIR Compiler: MegaCore® Function User Guide," version 3.3.0, rev. 1, pp. 3 11 through 3 15 (Oct. 2005). Altera Corporation, "FIR Compiler: MegaCore® Function User Guide," version 3.3.0, rev. 1, pp. 3 11 through 3 15 (Oct. 2005). Altera Corporation, "Advanced Synthesis Cookbook: A Design Guide for Stratix II, Stratix III and Stratix IV Devices," Document Version 3.0, 112 pgs., May 2008. Altera Corporation, "EIR Compiler: MegaCore® Function User Guide," version 3.3.0, rev. 1, pp. 3 11 through 3 15 (Oct. 2005). Altera Corporation, "FIR Compiler: MegaCore® Function User Guide," version 3.3.0, rev. 1, pp. 3 11 through 3 15 (Oct. 2005). Altera Corporation, "Advanced Synthesis Cookbook: A Design Guide for Stratix II, Stratix III and Stratix IV Devices," Document Version 3.0, 112 pgs., May 2008. Altera Corporation, "Advanced Synthesis Cookbook: A Design Guide for Stratix II, Stratix III and Stratix II and Stratix II of Str							
2009/0083358 A1 3/2009 Allen 2009/0113186 A1 4/2009 Kato et al. 2009/0172052 A1 7/2009 DeLaquil et al. 2009/0187615 A1 7/2009 Abe et al. 2009/0228689 A1 9/2009 Muff et al. 2010/0098189 A1 4/2010 Oketani 2010/0131577 A1 5/2010 Gangalakurti et al. 2010/0146022 A1 6/2010 Swartzlander et al. 2011/0161389 A1 6/2011 Langhammer et al. 2011/0219052 A1 9/2011 Langhammer et al. 2011/0238720 A1 9/2011 Langhammer et al. 2011/0320513 A1 12/2011 Langhammer et al. 2011/0054256 A1 3/2012 Langhammer 2012/0054256 A1 3/2012 Langhammer 2012/01540512 A1 6/2012 Wong et al. 2012/0166512 A1 6/2012 Wong et al. 2012/0191967 A1 7/2012 Lin et al.  Devices, "Štratix II Device Handbook, vol. 2, Chapter 6, v4.0 (Oct. 2005). Altera Corporation, "FIR Compiler: MegaCore® Function User Guide," version 3.3.0, rev. 1, pp. 3 11 through 3 15 (Oct. 2005). Altera Corporation, "Advanced Synthesis Cookbook: A Design Guide for Stratix II, Stratix III and Stratix IV Devices," Document Version 3.0, 112 pgs., May 2008. Amos, D., "PLD architectures match DSP algorithms," Electronic Product Design, vol. 17, No. 7, Jul. 1996, pp. 30, 32. Analog Devices, Inc., The Applications Engineering Staff of Analog Devices, DSP Division, Digital Signal Processing Applications Using the ADSP-2100 Family (edited by Amy Mar), 1990, pp. 141-192). Andrejas, J., et al., "Reusable DSP functions in FPGAs," Field-Programmable Logic and Applications. Roadmap to Reconfigurable Computing. 10th International Conference, FPL 2000. Proceedings (Lecture Notes in Computer Science vol. 1896) Aug. 27-30, 2000, pp. 456-461. Aoki, T., "Signed-weight arithmetic and its application to a field-programmable digital filter architecture," IEICE Transactions on							
2009/0172052 A1 7/2009 DeLaquil et al. 2009/0172052 A1 7/2009 DeLaquil et al. 2009/0187615 A1 7/2009 Abe et al. 2009/0228689 A1 9/2009 Muff et al. 2010/0098189 A1 4/2010 Oketani 2010/0131577 A1 5/2010 Gangalakurti et al. 2010/0191939 A1 7/2010 Muff et al. 2010/0191939 A1 7/2010 Muff et al. 2011/0219052 A1 9/2011 Langhammer et al. 2011/0238720 A1 9/2011 Langhammer et al. 2011/0320513 A1 12/2011 Langhammer 2012/0054256 A1 3/2012 Langhammer 2012/0054256 A1 3/2012 Langhammer 2012/01572 A1 6/2012 Shipgelblat 2012/0166512 A1 6/2012 Wong et al. 2012/0191967 A1 7/2012 Lin et al. 2009/0300088 A1 12/2009 Muff et al. 2009/0300088 A1 12/2009 Muff et al. 2010/031577 A1 5/2010 Gangalakurti et al. 2010/031577 A1 5/2010 Gangalakurti et al. 2010/031577 A1 5/2010 Swartzlander et al. 2010/046022 A1 6/2010 Swartzlander et al. 2010/054256 A1 3/2012 Langhammer 2011/0320513 A1 12/2011 Langhammer 2012/0054256 A1 3/2012 Langhammer 2012/0156512 A1 6/2012 Wong et al. 2012/0191967 A1 7/2012 Lin et al. 2008/300088 A1 12/2012 Abe et al. 2009/300088 A1 12/2013 Abe et al. Altera Corporation, "FIR Compiler: MegaCore® Function User Guide," version 3.3.0, rev. 1, pp. 31 1through 3 15 (Oct. 2005). Altera Corporation, "Advanced Synthesis Cookbook: A Design Guide," version 3.3.0, rev. 1, pp. 31 through 3 15 (Oct. 2005). Altera Corporation, "Advanced Synthesis Cookbook: A Design Guide," version 3.3.0, rev. 1, pp. 31 through 3 15 (Oct. 2005). Altera Corporation, "Advanced Synthesis Cookbook: A Design Guide," version 3.3.0, rev. 1, pp. 3 11 through 3 15 (Oct. 2005). Altera Corporation, "Advanced Synthesis Cookbook: A Design Guide," version 3.3.0, rev. 1, pp. 31 1 through 3 15 (Oct. 2005). Altera Corporation, "Advanced Synthesis Cookbook: A Design Guide," version 3.3.0, rev. 1, pp. 31 1 through 3.0 oct. Altera Corporation, "Advanced Synthesis Cookbook: A Design Guide," version 3.3.0, rev. 1, pp. 31 1 through 3.0, oct. Altera Corporation, "Advanced Synthesis Cookbook: A Design Guide, version 3.0, 12 pp. 2, 11 through 3.0, oct. Altera Corporation, "Advan							
2009/0172052 A1 7/2009 DeLaquil et al. 2009/0187615 A1 7/2009 Abe et al. 2009/0228689 A1 9/2009 Muff et al. 2009/0300088 A1 12/2009 Michaels et al. 2010/0098189 A1 4/2010 Oketani 2010/0131577 A1 5/2010 Gangalakurti et al. 2010/0146022 A1 6/2010 Muff et al. 2011/0161389 A1 6/2011 Langhammer et al. 2011/0238720 A1 9/2011 Langhammer et al. 2011/0320513 A1 12/2011 Langhammer 2011/0320513 A1 12/2011 Langhammer 2012/0054254 A1 3/2012 Langhammer 2012/0054256 A1 3/2012 Langhammer 2012/01540512 A1 6/2012 Wong et al. 2012/0166512 A1 6/2012 Wong et al. 2012/0191967 A1 7/2012 Lin et al.  Altera Corporation, "FIR Compiler: MegaCore® Function User Guide," version 3.3.0, rev. 1, pp. 3 11 through 3 15 (Oct. 2005). Altera Corporation, "Advanced Synthesis Cookbook: A Design Guide for Stratix II, Stratix III and Stratix IV Devices," Document Version 3.0, 112 pgs., May 2008. Amos, D., "PLD architectures match DSP algorithms," Electronic Product Design, vol. 17, No. 7, Jul. 1996, pp. 30, 32. Analog Devices, Inc., The Applications Engineering Staff of Analog Devices, DSP Division, Digital Signal Processing Applications Using the ADSP-2100 Family (edited by Amy Mar), 1990, pp. 141-192).  Andrejas, J., et al., "Reusable DSP functions in FPGAs," Field-Programmable Logic and Applications. Roadmap to Reconfigurable Computing. 10th International Conference, FPL 2000. Proceedings (Lecture Notes in Computer Science vol. 1896) Aug. 27-30, 2000, pp. 456-461.  Aoki, T., "Signed-weight arithmetic and its application to a field-programmable digital filter architecture," IEICE Transactions on						, ,	
2009/0228689 A1 9/2009 Muff et al. 2009/0300088 A1 12/2009 Michaels et al. 2010/0098189 A1 4/2010 Oketani 2010/0131577 A1 5/2010 Gangalakurti et al. 2010/0146022 A1 6/2010 Swartzlander et al. 2010/0191939 A1 7/2010 Muff et al. 2011/0161389 A1 6/2011 Langhammer et al. 2011/0238720 A1 9/2011 Langhammer et al. 2011/0320513 A1 12/2011 Langhammer 2012/0054254 A1 3/2012 Langhammer 2012/0054256 A1 3/2012 Langhammer 2012/013133 A1 5/2012 Shpigelblat 2012/0191967 A1 7/2012 Lin et al.  Altera Corporation, "Advanced Synthesis Cookbook: A Design Guide for Stratix II, Stratix III and Stratix IV Devices," Document Version 3.0, 112 pgs., May 2008.  Amos, D., "PLD architectures match DSP algorithms," Electronic Product Design, vol. 17, No. 7, Jul. 1996, pp. 30, 32.  Analog Devices, Inc., The Applications Engineering Staff of Analog Devices, DSP Division, Digital Signal Processing Applications Using the ADSP-2100 Family (edited by Amy Mar), 1990, pp. 141-192).  Andrejas, J., et al., "Reusable DSP functions in FPGAs," Field-Programmable Logic and Applications. Roadmap to Reconfigurable Computing. 10th International Conference, FPL 2000. Proceedings (Lecture Notes in Computer Science vol. 1896) Aug. 27-30, 2000, pp. 456-461.  Aoki, T., "Signed-weight arithmetic and its application to a field-programmable digital filter architecture," IEICE Transactions on	2009/0172052 A1						
2009/0300088 A1 12/2009 Mith et al. 2010/0098189 A1 12/2009 Michaels et al. 2010/0098189 A1 4/2010 Oketani 2010/0131577 A1 5/2010 Gangalakurti et al. 2010/0146022 A1 6/2010 Swartzlander et al. 2010/0191939 A1 7/2010 Muff et al. 2011/0161389 A1 6/2011 Langhammer et al. 2011/0219052 A1 9/2011 Langhammer 2011/0238720 A1 9/2011 Langhammer et al. 2011/0338720 A1 3/2012 Langhammer 2012/0054254 A1 3/2012 Langhammer 2012/0054254 A1 3/2012 Langhammer 2012/0054254 A1 3/2012 Langhammer 2012/013133 A1 5/2012 Shpigelblat 2012/0166512 A1 6/2012 Wong et al. 2012/0191967 A1 7/2012 Lin et al.  Guide for Stratix II, Stratix III and Stratix IV Devices," Document Version 3.0, 112 pgs., May 2008. Amos, D., "PLD architectures match DSP algorithms," Electronic Product Design, vol. 17, No. 7, Jul. 1996, pp. 30, 32. Analog Devices, Inc., The Applications Engineering Staff of Analog Devices, DSP Division, Digital Signal Processing Applications Using the ADSP-2100 Family (edited by Amy Mar), 1990, pp. 141-192). Andrejas, J., et al., "Reusable DSP functions in FPGAs," Field-Programmable Logic and Applications. Roadmap to Reconfigurable Computing. 10th International Conference, FPL 2000. Proceedings (Lecture Notes in Computer Science vol. 1896) Aug. 27-30, 2000, pp. 456-461. Aoki, T., "Signed-weight arithmetic and its application to a field-programmable digital filter architecture," IEICE Transactions on	2009/0187615 A1	7/2009	Abe et al.				
2010/0098189 A1 4/2010 Oketani 2010/0131577 A1 5/2010 Gangalakurti et al. 2010/0146022 A1 6/2010 Swartzlander et al. 2010/0146039 A1 7/2010 Muff et al. 2011/0161389 A1 6/2011 Langhammer et al. 2011/0219052 A1 9/2011 Langhammer et al. 2011/0320513 A1 12/2011 Langhammer 2012/0054254 A1 3/2012 Langhammer 2012/0054256 A1 3/2012 Langhammer 2012/0054256 A1 3/2012 Langhammer 2012/0054256 A1 5/2012 Shpigelblat 2012/0166512 A1 6/2012 Wong et al. 2012/0166512 A1 6/2012 Wong et al. 2012/0191967 A1 7/2012 Michaets et al. Version 3.0, 112 pgs., May 2008. Amos, D., "PLD architectures match DSP algorithms," Electronic Product Design, vol. 17, No. 7, Jul. 1996, pp. 30, 32. Analog Devices, Inc., The Applications Engineering Staff of Analog Devices, DSP Division, Digital Signal Processing Applications Using the ADSP-2100 Family (edited by Amy Mar), 1990, pp. 141-192). Analog Devices, DSP Division, Digital Signal Processing Applications Using the ADSP-2100 Family (edited by Amy Mar), 1990, pp. 141-192). Analog Devices, Inc., The Applications Engineering Staff of Analog Devices, DSP Division, Digital Signal Processing Applications Using the ADSP-2100 Family (edited by Amy Mar), 1990, pp. 141-192). Analog Devices, Inc., The Applications Engineering Staff of Analog Devices, DSP Division, Digital Signal Processing Applications Using the ADSP-2100 Family (edited by Amy Mar), 1990, pp. 141-192). Analog Devices, DSP Division, Digital Signal Processing Applications Using the ADSP-2100 Family (edited by Amy Mar), 1990, pp. 141-192). Analog Devices, Inc., The Applications Engineering Staff of Analog Devices, DSP Division, Digital Signal Processing Applications Using the ADSP-2100 Family (edited by Amy Mar), 1990, pp. 141-192). Analog Devices, DSP Division, Digital Signal Processing Applications Computer Science vol. 1896 Aug. 27-30, 2000, pp. 401-192). Analog Devices, DSP Division, Digital Signal Processing Applications Computer Science vol. 1896 Aug. 27-30, 2000, pp. 401-192). Analog Devices, DSP Division, Digital Signal Processing Applic	2009/0228689 A1	9/2009	Muff et al.				
2010/0098189 Al 4/2010 Oketani 2010/0131577 Al 5/2010 Gangalakurti et al. 2010/0146022 Al 6/2010 Swartzlander et al. 2010/0191939 Al 7/2010 Muff et al. 2011/0161389 Al 6/2011 Langhammer et al. 2011/0238720 Al 9/2011 Langhammer et al. 2011/0320513 Al 12/2011 Langhammer 2012/0054254 Al 3/2012 Langhammer 2012/0054256 Al 3/2012 Langhammer 2012/0054256 Al 3/2012 Langhammer 2012/013133 Al 5/2012 Shpigelblat 2012/0166512 Al 6/2012 Wong et al. 2012/0191967 Al 7/2012 Lin et al.  Amos, D., "PLD architectures match DSP algorithms," Electronic Product Design, vol. 17, No. 7, Jul. 1996, pp. 30, 32. Analog Devices, Inc., The Applications Engineering Staff of Analog Devices, DSP Division, Digital Signal Processing Applications Using the ADSP-2100 Family (edited by Amy Mar), 1990, pp. 141-192).  Analog Devices, DSP Division, Digital Signal Processing Applications Using the ADSP-2100 Family (edited by Amy Mar), 1990, pp. 141-192).  Andrejas, J., et al., "Reusable DSP functions in FPGAs," Field-Programmable Logic and Applications. Roadmap to Reconfigurable Computing. 10th International Conference, FPL 2000. Proceedings (Lecture Notes in Computer Science vol. 1896) Aug. 27-30, 2000, pp. 456-461.  Aoki, T., "Signed-weight arithmetic and its application to a field-programmable digital filter architecture," IEICE Transactions on	2009/0300088 A1	12/2009	Michaels et al.				ices, Document
2010/0131577 Al 5/2010 Gangalakurft et al. 2010/0146022 Al 6/2010 Swartzlander et al. 2010/0191939 Al 7/2010 Muff et al. 2011/0161389 Al 6/2011 Langhammer et al. 2011/0219052 Al 9/2011 Langhammer et al. 2011/03238720 Al 9/2011 Langhammer et al. 2011/0320513 Al 12/2011 Langhammer 2012/0054254 Al 3/2012 Langhammer 2012/0054256 Al 3/2012 Langhammer 2012/0054256 Al 5/2012 Shpigelblat 2012/013133 Al 5/2012 Shpigelblat 2012/0166512 Al 6/2012 Wong et al. 2012/0191967 Al 5/2010 Gangalakurft et al. Product Design, vol. 17, No. 7, Jul. 1996, pp. 30, 32. Analog Devices, Inc., The Applications Engineering Staff of Analog Devices, DSP Division, Digital Signal Processing Applications Using the ADSP-2100 Family (edited by Amy Mar), 1990, pp. 141-192). Andrejas, J., et al., "Reusable DSP functions in FPGAs," Field-Programmable Logic and Applications. Roadmap to Reconfigurable Computing. 10th International Conference, FPL 2000. Proceedings (Lecture Notes in Computer Science vol. 1896) Aug. 27-30, 2000, pp. 456-461. 2012/0191967 Al 7/2012 Lin et al.	2010/0098189 A1						hms." Electronic
2010/0191939 A1 7/2010 Muff et al. Devices, DSP Division, Digital Signal Processing Applications 2011/0161389 A1 6/2011 Langhammer et al. 2011/0219052 A1 9/2011 Langhammer et al. 2011/0238720 A1 9/2011 Langhammer et al. 2011/0320513 A1 12/2011 Langhammer et al. 2012/054254 A1 3/2012 Langhammer 2012/0054256 A1 3/2012 Langhammer 2012/0054256 A1 3/2012 Langhammer 2012/013133 A1 5/2012 Shpigelblat 456-461. 2012/0191967 A1 7/2012 Lin et al. Park Applications In FAGAs, The Applications In English and Standard Processing Applications Using the ADSP-2100 Family (edited by Amy Mar), 1990, pp. 141-192). Andrejas, J., et al., "Reusable DSP functions in FPGAs," Field-Programmable Logic and Applications. Roadmap to Reconfigurable Computing. 10th International Conference, FPL 2000. Proceedings (Lecture Notes in Computer Science vol. 1896) Aug. 27-30, 2000, pp. 2012/016512 A1 6/2012 Wong et al. Aoki, T., "Signed-weight arithmetic and its application to a field-programmable digital filter architecture," IEICE Transactions on			_				
2011/0161389 A1 6/2011 Langhammer et al. Using the ADSP-2100 Family (edited by Amy Mar), 1990, pp. 141-2011/0238720 A1 9/2011 Langhammer et al. 2011/0320513 A1 12/2011 Langhammer et al. 2012/0054254 A1 3/2012 Langhammer 2012/0054256 A1 3/2012 Langhammer 2012/0054256 A1 3/2012 Langhammer 2012/013133 A1 5/2012 Shpigelblat 456-461. 2012/0166512 A1 6/2012 Wong et al. 2012/0191967 A1 7/2012 Lin et al. Using the ADSP-2100 Family (edited by Amy Mar), 1990, pp. 141-1920. Andrejas, J., et al., "Reusable DSP functions in FPGAs," Field-Programmable Logic and Applications. Roadmap to Reconfigurable Computing. 10th International Conference, FPL 2000. Proceedings (Lecture Notes in Computer Science vol. 1896) Aug. 27-30, 2000, pp. 456-461. Aoki, T., "Signed-weight arithmetic and its application to a field-programmable digital filter architecture," IEICE Transactions on				Analo	g Devices, Inc., The App	olications Engineerin	g Staff of Analog
2011/0219052 A1 9/2011 Langhammer 192). 2011/0238720 A1 9/2011 Langhammer et al. Andrejas, J., et al., "Reusable DSP functions in FPGAs," Field-2011/0320513 A1 12/2011 Langhammer 2012/0054254 A1 3/2012 Langhammer 2012/0054256 A1 3/2012 Langhammer 2012/0054256 A1 3/2012 Langhammer 2012/0113133 A1 5/2012 Shpigelblat 456-461. 2012/0166512 A1 6/2012 Wong et al. Andrejas, J., et al., "Reusable DSP functions in FPGAs," Field-Programmable Logic and Applications. Roadmap to Reconfigurable Computing. 10th International Conference, FPL 2000. Proceedings (Lecture Notes in Computer Science vol. 1896) Aug. 27-30, 2000, pp. 436-461. 2012/0191967 A1 7/2012 Lin et al. Aoki, T., "Signed-weight arithmetic and its application to a field-programmable digital filter architecture," IEICE Transactions on				Devic	es, DSP Division, Dig	ital Signal Processi	ing Applications
2011/0238720 A1 9/2011 Langhammer et al. Andrejas, J., et al., "Reusable DSP functions in FPGAs," Field- 2011/0320513 A1 12/2011 Langhammer  2012/0054254 A1 3/2012 Langhammer  2012/0054256 A1 3/2012 Langhammer  2012/013133 A1 5/2012 Shpigelblat  2012/0166512 A1 6/2012 Wong et al.  2012/0191967 A1 7/2012 Lin et al. Andrejas, J., et al., "Reusable DSP functions in FPGAs," Field- Programmable Logic and Applications. Roadmap to Reconfigurable  Computing. 10th International Conference, FPL 2000. Proceedings  (Lecture Notes in Computer Science vol. 1896) Aug. 27-30, 2000, pp.  456-461.  Aoki, T., "Signed-weight arithmetic and its application to a field- programmable digital filter architecture," IEICE Transactions on			•	_	the ADSP-2100 Family	(edited by Amy Mar	), 1990, pp. 141-
2011/0320513 A1 12/2011 Langhammer Programmable Logic and Applications. Roadmap to Reconfigurable Computing. 10th International Conference, FPL 2000. Proceedings (Lecture Notes in Computer Science vol. 1896) Aug. 27-30, 2000, pp. 2012/0113133 A1 5/2012 Shpigelblat 456-461. 2012/0166512 A1 6/2012 Wong et al. Aoki, T., "Signed-weight arithmetic and its application to a field-programmable digital filter architecture," IEICE Transactions on			•				
2012/0054254 A1 3/2012 Langhammer Computing. 10th International Conference, FPL 2000. Proceedings (Lecture Notes in Computer Science vol. 1896) Aug. 27-30, 2000, pp. 2012/0113133 A1 5/2012 Shpigelblat 456-461. 2012/0166512 A1 6/2012 Wong et al. Aoki, T., "Signed-weight arithmetic and its application to a field-programmable digital filter architecture," IEICE Transactions on							
2012/0054256 A1 3/2012 Langhammer (Lecture Notes in Computer Science vol. 1896) Aug. 27-30, 2000, pp. 2012/0113133 A1 5/2012 Shpigelblat 456-461. 2012/0166512 A1 6/2012 Wong et al. Aoki, T., "Signed-weight arithmetic and its application to a field-programmable digital filter architecture," IEICE Transactions on							
2012/0113133 A1 5/2012 Shpigelblat 456-461. 2012/0166512 A1 6/2012 Wong et al. 2012/0191967 A1 7/2012 Lin et al.  5/2012 Shpigelblat 456-461.  Aoki, T., "Signed-weight arithmetic and its application to a field-programmable digital filter architecture," <i>IEICE Transactions on</i>							
2012/0166512 A1 6/2012 Wong et al. Aoki, T., "Signed-weight arithmetic and its application to a field-2012/0191967 A1 7/2012 Lin et al. Aoki, T., "Signed-weight arithmetic and its application to a field-programmable digital filter architecture," <i>IEICE Transactions on</i>			-	,	*	ience voi. 1090) Aug.	. 27-30, 2000, pp.
2012/0191967 A1 7/2012 Lin et al. programmable digital filter architecture," <i>IEICE Transactions on</i>						hmetic and its applic	cation to a field-
	2012/0290819 A1	11/2012	Langhammer	Electr	onics, 1999 , vol. E82C.	No. 9, Sep. 1999, pp	o. 1687 <b>-</b> 1698.

### (56) References Cited

### OTHER PUBLICATIONS

Ashour, M.A., et al., "An FPGA implementation guide for some different types of serial-parallel multiplier-structures," *Microelectronics Journal*, vol. 31, No. 3, 2000, pp. 161-168.

Berg, B.L., et al. "Designing Power and Area Efficient Multistage FIR Decimators with Economical Low Order Filters," *ChipCenter Technical Note*, Dec. 2001.

Bursky, D., "Programmable Logic Challenges Traditional ASIC SoC Designs", *Electronic Design*, Apr. 15, 2002.

Chhabra, A. et al., Texas Instruments Inc., "A Block Floating Point Implementation on the TMS320C54x DSP", Application Report SPRA610, Dec. 1999, pp. 1-10.

Colet, P., "When DSPs and FPGAs meet: Optimizing image processing architectures," *Advanced Imaging*, vol. 12, No. 9, Sep. 1997, pp. 14, 16, 18.

Crookes, D., et al., "Design and implementation of a high level programming environment for FPGA-based image processing," *IEE Proceedings-Vision, Image and Signal Processing*, vol. 147, No. 4, Aug. 2000, pp. 377-384.

Debowski, L., et al., "A new flexible architecture of digital control systems based on DSP and complex CPLD technology for power conversion applications," *PCIM 2000: Europe Official Proceedings of the Thirty-Seventh International Intelligent Motion Conference*, Jun. 6-8, 2000, pp. 281-286.

de Dinechin, F. et al., "Large multipliers with less DSP blocks," retrieved from http://hal-ens-lyon.archives-ouvertes.fr/ensl-00356421/en/, 9 pgs., available online Jan. 2009.

de Dinechin F., et al., "FPGA-Specific Custom Arithmetic Datapath Design: LIP Research Report RR2010-34," Dec. 2010, 8 pages.

Dick, C., et al., "Configurable logic for digital communications: some signal processing perspectives," *IEEE Communications Magazine*, vol. 37, No. 8, Aug. 1999, pp. 107-111.

Do, T.-T., et al., "A flexible implementation of high-performance FIR filters on Xilinx FPGAs," Field-Programmable Logic and Applications: From FPGAs to Computing Paradigm. 8th International Workshop, FPL'98. Proceedings, Hartenstein, R.W., et al., Aug.-Sep. 3, 1998, pp. 441-445.

Farooqui, A., et al., "General Data-Path Organization of a MAC unit for VLSI Implementation of DSP Processors," ISCAS '98, Part 2, May 31, 1998-Jun. 3, 1998, pp. 260-263.

Fujioka, Y., et al., "240 MOPS Reconfigurable Parallel VLSI Processor for Robot Control", Proceedings of the 1992 International Conference on Industrial Electronics, Control, Instrumentation, and Automation, vol. 3, pp. 1385-1390, Nov. 9-13, 1992.

Gaffer, A.A., et al., "Floating-Point Bitwidth Analysis via Automatic Differentiation," *IEEE Conference on Field Programmable Technology*, Hong Kong, Dec. 2002.

Govindu, G. et al., "A Library of Parameterizable Floating-Point Cores for FPGAs and Their Application to Scientific Computing," *Proc Int'l Conf. Eng. Reconfigurable Systems and Algorithms* (ERSA'05), Jun. 2005.

Govindu, G. et al., "Analysis of High-performance Floating-point Arithmetic on FPGAs," *Proceedings of the 18th International Parallel and Distributed Processing Symposium* (PDPS'04) pp. 149-156, Apr. 2004.

Guccione, S.A., "Run-time Reconfiguration at Xilinx," *Parallel and distributed processing: 15 IPDPS 2000 workshops*, Rolim, J., ed., May 1-5, 2000, p. 873.

Hauck, S., "The Future of Reconfigurable Systems," *Keynote Address, 5th Canadian Conference on Field Programmable Devices*, Jun. 1998, http:--.www.ee.washington.edu-people-faculty-hauck-publications-ReconfigFuture.PDF.

Haynes, S.D., et al., "Configurable multiplier blocks for embedding in FPGAs," *Electronicas Letters*, vol. 34, No. 7, pp. 638-639 (Apr. 2, 1998).

Heysters, P.M., et al., "Mapping of DSP algorithms on field programmable function arrays," Field-Programmable Logic and Applications. Roadmap to Reconfigurable Computing. 10th International Conference, FPL 2000, Proceedings (Lecture Notes in Computer Science vol. 1896) Aug. 27-30, 2000, pp. 400-411.

Huang, J., et al., "Simulated Performance of 1000BASE-T Receiver with Different Analog Front End Designs," *Proceedings of the 35th Asilomar Conference on Signals, Systems, and Computers*, Nov. 4-7, 2001.

IEEE Standard for Binary Floating-Point Arithmetic, *ANSI/IEEE Standard*, Std 754, 1985, pp. 1-14.

IEEE Standard for Floating-Point Arithmetic, *IEEE Std 754*, 2008, pp. 1-58.

"Implementing Multipliers in FLEX 10K EABs", *Altera*, Mar. 1996. "Implementing Logic with the Embedded Array in Flex 10K Devices", *Altera*, May 2001, ver. 2.1.

Jinghua Li, "Design a pocket multi-bit multiplier in FPGA," 1996 2nd International Conference on ASIC Proceedings (IEEE Cat. No. 96TH8140) Oct. 21-24, 1996, pp. 275-279.

Jones, G., "Field-programmable digital signal conditioning," *Electronic Product Design*, vol. 21, No. 6, Jun. 2000, pp. C36-C38.

Karlstrom, K., et al., "High Performance, Low Latency FPGA based Floating Point Adder and Multiplier Units in a Virtex 4," Norchip Conf., pp. 31-34, 2006.

Kiefer, R., et al., "Performance comparison of software-FPGA hardware partitions for a DSP application" 14th Australian Microelectronics Conference, Microelectronics: Technology Today for the Future, MICRO '97 Proceedings, Sep. 28-Oct. 1, 1997, pp. 88-93. Kim, Y., et al., "Fast GPU Implementation for the Solution of

Kim, Y., et al., "Fast GPU Implementation for the Solution of Tridiagonal Matrix Systems," *Journal of Korean Institute of Information Scientists and Engineers*, vol. 32, No. 12, pp. 692-704, Dec. 2005.

Kramberger, I., "DSP acceleration using a reconfigurable FPGA," *ISIE '99.Proceedings of the IEEE International Symposium on Industrial Electronics* (Cat.No. 99TH8465), vol. 3, Jul. 12-16, 1999, pp. 1522-1525.

Langhammer, M., "How to implement DSP in programmable logic," *Elettronica Oggi*, No. 266, Dec. 1998, pp. 113-115.

Langhammer, "Floating Point Datapath Synthesis for FPGAs," *IEEE International Conference on Field Programmable Logic and Applications*, 2008 (FPL 2008), pp. 355-360 (Sep. 8-10, 2008).

Langhammer, M., "Implementing a DSP in Programmable Logic," *Online EE Times*, May 1998, http:--www.eetimes.com-editorial-1998-coverstory9805.html.

Lazaravich, B.V., "Function block oriented field programmable logic arrays," *Motorola, Inc. Technical Developments*, vol. 18, Mar. 1993, pp. 10-11.

Lattice Semiconductor Corp, ORCA® FPGA Express™ Interface Manual: ispLEVER® Version 3.0, 2002.

Lucent Technologies, Microelectronics Group, "Implementing and Optimizing Multipliers in ORCA<sup>TM</sup> FPGAs,", Application Note. AP97-008FGPA, Feb. 1997.

Lund, D., et al., "A new development system for reconfigurable digital signal processing," First International Conference on 3G Mobile Communication Technologies (Conf. Publ. No. 471), Mar. 27-29, 2000, pp. 306-310.

Martinson, L. et al., "Digital matched Filtering with Pipelined Floating Point Fast Fourier Transforms (FFT's)," *IEEE Transactions on Acoustics, Speech, and Signal Processing*, vol. ASSP-23, No. 2, pp. 222-234, Apr. 1975.

Miller, N.L., et al., "Reconfigurable integrated circuit for high performance computer arithmetic," *Proceedings of the 1998 IEE Colloquium on Evolvable Hardware Systems (Digest)*, No. 233, 1998, pp. 2-1-2-4.

Mintzer, L., "Xilinx FPGA as an FFT processor," *Electronic Engineering*, vol. 69, No. 845, May 1997, pp. 81, 82, 84.

Faura et al., "A Novel Mixed Signal Programmable Device With On-Chip Microprocessor," Custom Integrated Circuits Conference, 1997. Proceedings of the IEEE 1997 Santa Clara, CA, USA, May 5, 1997, pp. 103-106.

Nakasato, N., et al., "Acceleration of Hydrosynamical Simulations using a FPGA board", *The Institute of Electronics Information and Communication Technical Report CPSY2005-47*, vol. 105, No. 515, Jan. 17, 2006.

Nedjah, N., et al., "Fast Less Recursive Hardware for Large Number Multiplication Using Karatsuba-Ofman's Algorithm," *Computer and Information Sciences—ISCIS*, pp. 43-50, 2003.

### (56) References Cited

### OTHER PUBLICATIONS

Nozal, L., et al., "A new vision system: programmable logic devices and digital signal processor architecture (PLD+FDSP)," *Proceedings IECON '91. 1991 International Conference on Industrial Electronics, Control and Instrumentation* (Cat. No. 91CH2976-9) vol. 3, Oct. 28-Nov. 1, 1991, pp. 2014-2018.

Osana, Y., et al., "Hardware-resource Utilization Analysis on an FPGA-Based Biochemical Simulator ReCSiP", *The Institute of Electronics Information and Communication Technical Report CPSY2005-63*, vol. 105, No. 516, Jan. 18, 2006.

Papenfuss, J.R, et al., "Implementation of a real-time, frequency selective, RF channel simulator using a hybrid DSP-FPGA architecture," *RAWCON 2000: 2000 IEEE Radio and Wireless Conference* (Cat. No. 00EX404), Sep. 10-13, 2000, pp. 135-138.

Parhami, B., "Configurable arithmetic arrays with data-driven control," 34th Asilomar Conference on Signals, Systems and Computers, vol. 1, 2000, pp. 89-93.

"The QuickDSP Design Guide", Quicklogic, Aug. 2001, revision B. "QuickDSP™ Family Data Sheer", *Quicklogic*, Aug. 7, 2001, revision B.

Rangasayee, K., "Complex PLDs let you produce efficient arithmetic designs," *EDN (European Edition)* vol. 41, No. 13, Jun. 20, 1996, pp. 109, 110, 112, 114, 116.

Rosado, A., et al., "A high-speed multiplier coprocessor unit based on FPGA," *Journal of Electrical Engineering*, vol. 48, No. 11-12, 1997, pp. 298-302.

Santillan-Q., G.F., et al., "Real-time integer convolution implemented using systolic arrays and a digit-serial architecture in complex programmable logic devices," *Proceedings of the Third International Workshop on Design of Mixed-Mode Integrated Circuits and Applications* (Cat. No.99EX303) Jul. 26-28, 1999, pp. 147-150.

Texas Instruments Inc., "TMS320C54x DSP Reference Set, vol. 1: CPU and Peripherals", Literature No. SPRU131F, Apr. 1999, pp. 2-1 through 2-16 and 4-1 through 4-29.

Thapliyal, H., et al., "Combined Integer and Floating Point Multiplication Architecture (CIFM) for FPGSs and Its Reversible Logic Implementation", *Proceedings MWSCAS 2006*, Puerto Rico, 5 pages, Aug. 2006.

Thapliyal, H., et al., "Combined Integer and Variable Precision (CIVP) Floating Point Multiplication Architecture for FPGAs", *Proceedings of the 2007 International Conference on Parallel and Distributed Processing Techniques and Applications (PDPTA'07)*, Las Vegas, US, vol. 1, pp. 449-450, Jun. 2007.

Tisserand, A., et al., "An on-line arithmetic based FPGA for low power custom computing," Field Programmable Logic and Applications, 9th International Workshop, FPL'99, Proceedings (Lecture Notes in Computer Science vol. 1673), Lysaght, P., et al., eds., Aug. 30-Sep. 1, 1999, pp. 264-273.

Tralka, C., "Symbiosis of DSP and PLD," *Elektronik*, vol. 49, No. 14, Jul. 11, 2000, pp. 84-96.

Underwood, K. "FPGAs vs. CPUs: Trends in Peak Floating-Point Performance," *Proceedings of the 2004 ACM-SIGDA 12th International Symposium on Field Programmable Gate Arrays*, pp. 171-180, Feb. 22-24, 2004.

Valls, J., et al., "A Study About FPGA-Based Digital Filters," Signal Processing Systems, 1998, SIPS 98, 1998 IEEE Workshop, Oct. 10, 1998, pp. 192-201.

"Virtex-II 1.5V Field-Programmable Gate Arrays", *Xilinx*, Jan. 25, 2001, module 2 of 4.

"Virtex-II 1.5V Field-Programmable Gate Arrays", *Xilinx*, Apr. 2, 2001, module 1 of 4.

"Virtex-II 1.5V Field-Programmable Gate Arrays", *Xilinx*, Apr. 2, 2001, module 2 of 4.

Vladimirova, T. et al., "Floating-Point Mathematical Co-Processor for a Single-Chip On-Board Computer," *MAPLD'03 Conference*, *D5*, Sep. 2003.

Wajih, E.-H.Y. et al., "Efficient Hardware Architecture of Recursive Karatsuba-Ofman Multiplier," 3<sup>rd</sup> International Conference on Design and Technology of Integrated Systems in Nanoscale Era, 6 pgs, Mar. 2008.

Walters, A.L., "A Scaleable Fir Filter Implementation Using 32-bit Floating-Point Complex Arithmetic on a FPGA Based Custom Computing Platform," Allison L. Walters, Thesis Submitted to the Faculty of Virginia Polytechnic Institute and State University, Jan. 30, 1998. Weisstein, E.W., "Karatsuba Multiplication," *MathWorld—A Wolfram Web Resource* (Dec. 9, 2007), accessed Dec. 11, 2007 at http:--. mathworld.wolfram.com-KaratsubaMultiplication.html.

Wenzel, L., "Field programmable gate arrays (FPGAs) to replace digital signal processor integrated circuits," *Elektronik*, vol. 49, No. 5, Mar. 7, 2000, pp. 78-86.

"Xilinx Unveils New FPGA Architecture to Enable High-Performance, 10 Million System Gate Designs", Xilinx, Jun. 22, 2000.

"Xilinx Announces DSP Algorithms, Tools and Features for Virtex-II Architecture", *Xilinx*, Nov. 21, 2000.

Xilinx Inc., "Virtex-II 1.5V Field-Programmable Gate Arrays", Advance Product Specification, DS031-2 (v1.9), Nov. 29, 2001, Module 2 of 4, pp. 1-39.

Xilinx Inc., "Using Embedded Multipliers", Virtex-II Platform FPGA Handbook, UG002 (v1.3), Dec. 3, 2001, pp. 251-257.

Xilinx, Inc., "A 1D Systolic FIR," copyright 1994-2002, downloaded from http:--www.iro.umontreal.ca-~aboulham-F6221-Xilinx%20A%201D%20systolic%20FIR.htm.

Xilinx, Inc., "The Future of FPGA's," White Paper, available Nov. 14, 2005 for download from http:--www.xilinx.com-prs\_rls,5yrwhite. htm.

Xilinx Inc., "XtremeDSP Design Considerations User Guide," v 1.2, Feb. 4, 2005.

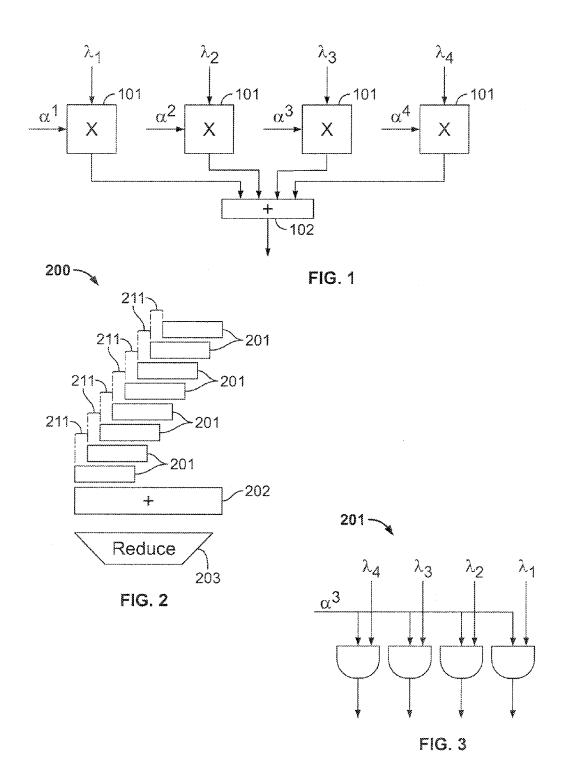
Xilinx Inc., "Complex Multiplier v2.0", DS291 Product Specification/Datasheet, Nov. 2004.

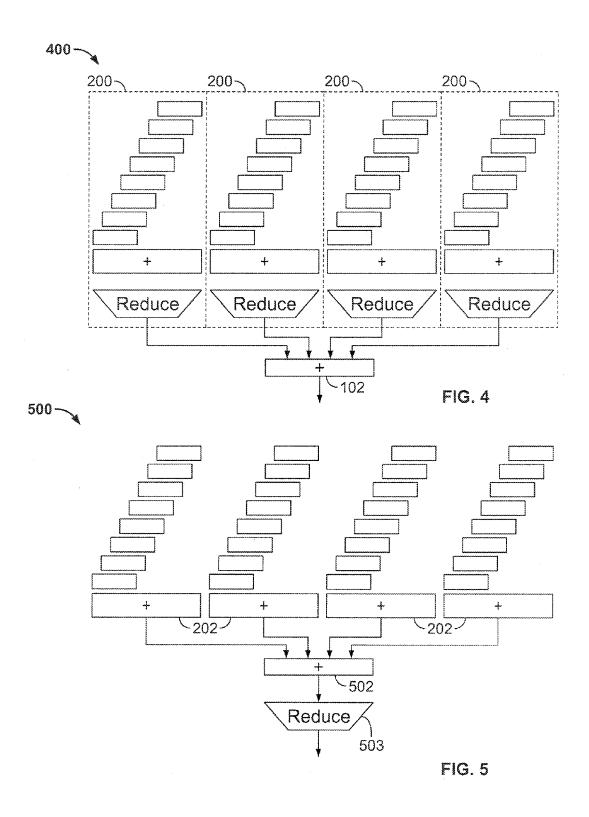
Xilinx, Inc., "Virtex-5 ExtremeDSP Design Considerations," *User Guide UG193*,v2.6, 114 pages, Oct. 2007.

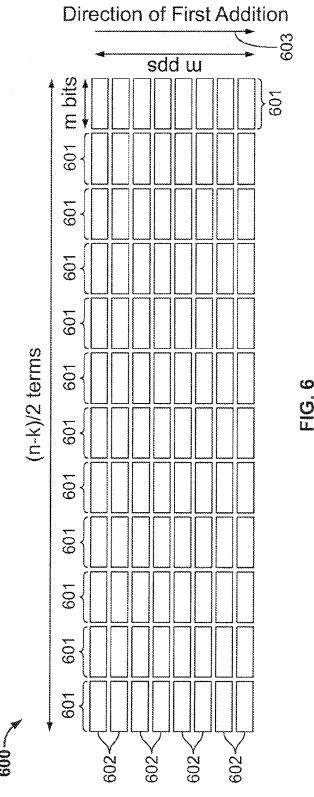
Xilinx, Inc., "Implementing Barrel Shifters Using Multipliers", p. 1-4, Aug. 17, 2004.

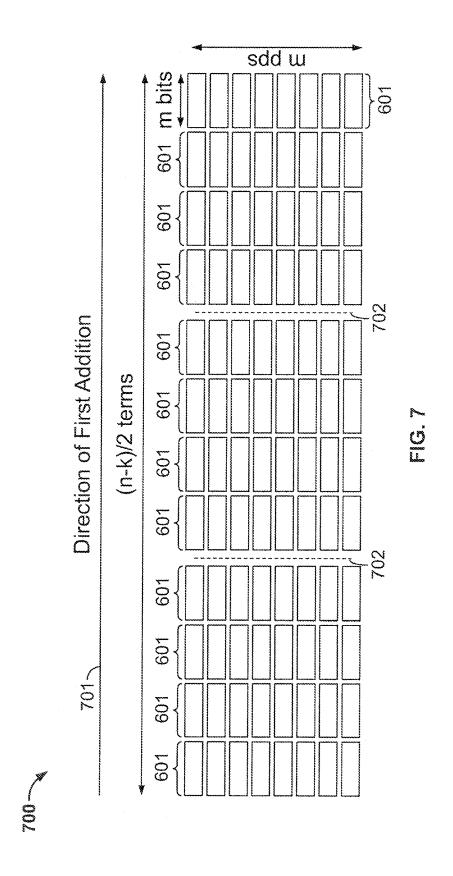
Zhou, G. et al., "Efficient and High-Throughput Implementations of AES-GCM on FPGAs," *International Conference on Field-Programmable Technology*, 8 pgs., Dec. 2007.

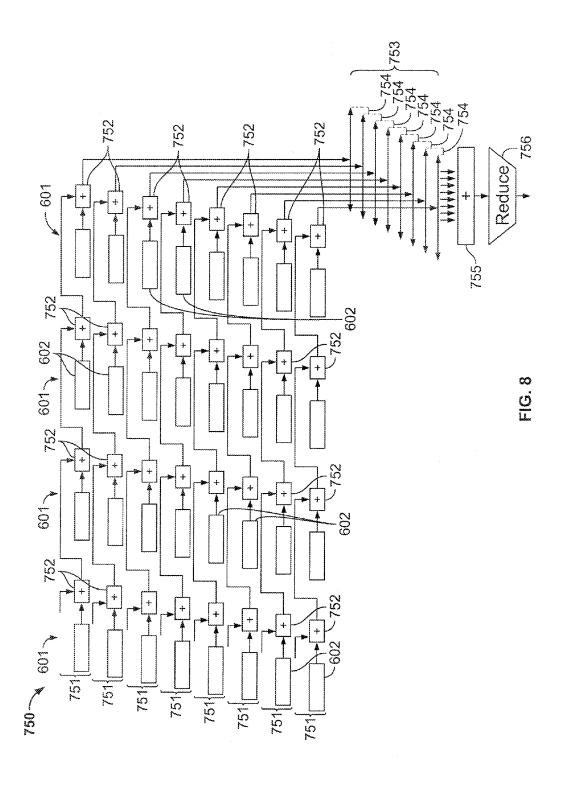
\* cited by examiner

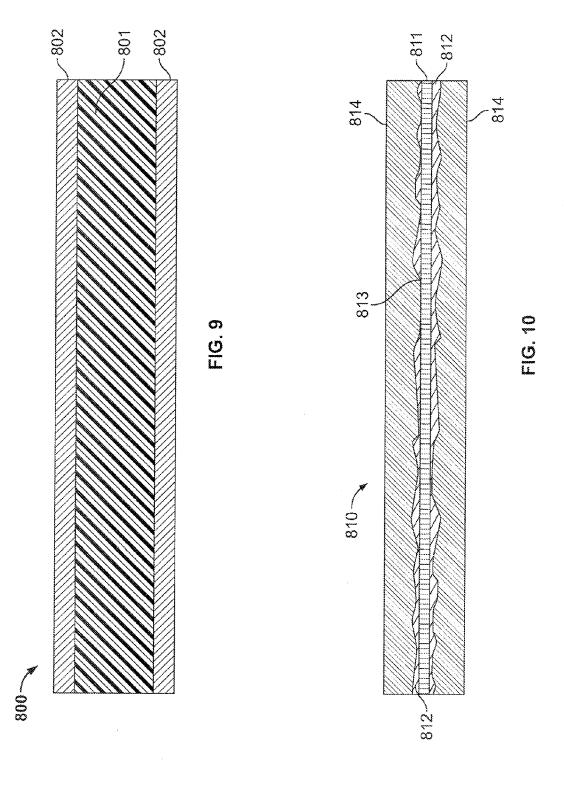












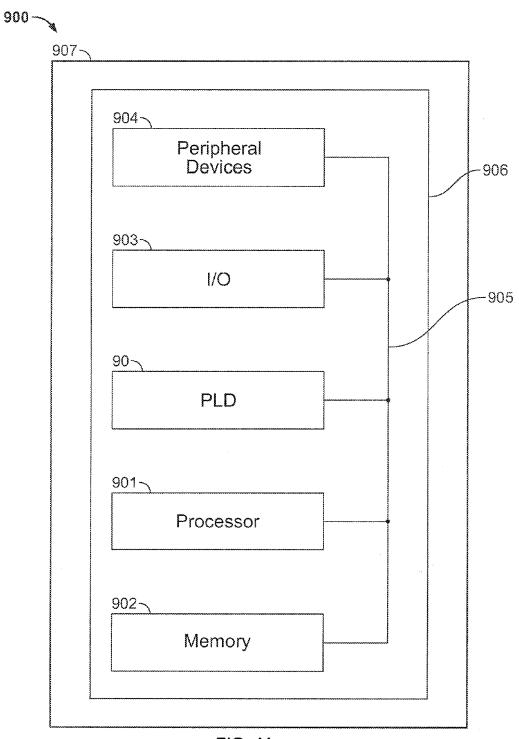


FIG. 11

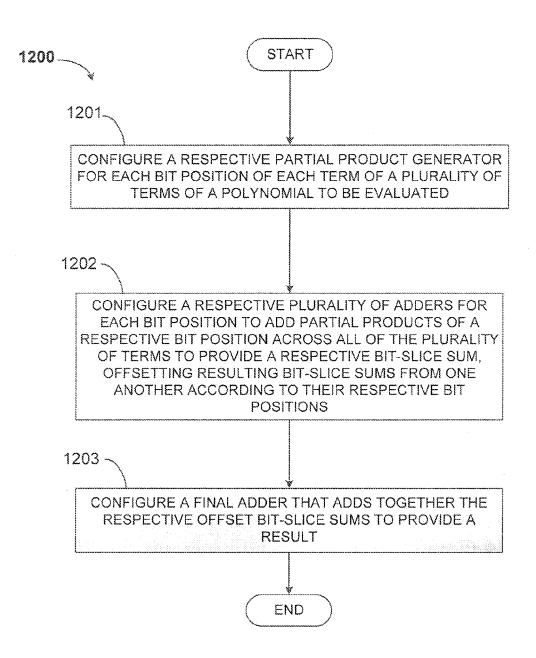


FIG. 12

### POLYNOMIAL CALCULATIONS OPTIMIZED FOR PROGRAMMABLE INTEGRATED CIRCUIT DEVICE STRUCTURES

### CROSS REFERENCE TO RELATED APPLICATION

This claims the benefit of commonly-assigned U.S. Provisional Patent Application No. 61/729,797, filed Nov. 26, 2012, which is hereby incorporated by reference herein in its entirety.

#### FIELD OF THE INVENTION

This invention relates to computing floating-point polynomials in programmable integrated circuit devices such as programmable logic devices (PLDs).

### BACKGROUND OF THE INVENTION

Certain operations, such as certain memory operations, 20 embodiment of the present invention; require evaluation of multiple shifted instances of the same polynomials. This is commonly done by adding multiple shifted partial products for each term, and then adding together all of those sums. However, such an operation may be inefficient when implemented in certain types of devices, 25 particularly in programmable devices such as field-programmable gate arrays (FPGAs) that perform logic operations using arrangements of look-up tables (LUTs). In particular, because at or near both the most-significant bit and the least significant bit there are many empty positions, the addition 30 operations do not pack efficiently into the LUTs.

### SUMMARY OF THE INVENTION

The present invention relates to method and circuitry for 35 implementing polynomial calculations using logic structures such as those found in programmable devices such as FPGAs. Instead of summing all of the partial products for each respective multiplier, and then adding together those sums, the partial products are summed across all multipliers in a bit- 40 slice-by-bit-slice order. The sums of the bit slices are then in turn shifted by their relative indices and summed, and then reduced as necessary. Because the initial addition is across a bit slice, all bit positions within the sum will have similar hamming count—i.e., will be similarly populated. Therefore, 45 the sums will pack efficiently into LUTs. Moreover, any level of pipelining can be used.

In accordance with embodiments of the invention, there is provided polynomial circuitry including a respective partial product generator for each bit position of each term of a 50 plurality of terms of a polynomial to be evaluated. A respective plurality of adders for each bit position adds partial products of a respective bit position across all of the plurality of terms to provide a respective bit-slice sum. Resulting bit-slice sums are offset from one another according to their respective 55 bit positions. A final adder adds together the respective offset bit-slice sums to provide a result.

A method of configuring a programmable device as such polynomial circuitry is also provided, and a non-transitory machine-readable data storage medium is provided that is 60 encoded with software for performing the method of configuring such circuitry on a programmable device.

### BRIEF DESCRIPTION OF THE DRAWINGS

Further features of the invention, its nature and various advantages will be apparent upon consideration of the follow2

ing detailed description, taken in conjunction with the accompanying drawings, in which like reference characters refer to like parts throughout, and in which:

FIG. 1 shows a conceptual arrangement for evaluating shifted polynomials;

FIG. 2 shows schematically a circuit arrangement that can serve as one of the multipliers in FIG. 1:

FIG. 3 shows schematically a circuit arrangement that can serve as one of the partial product generators in FIG. 2;

FIG. 4 shows a circuit arrangement in which the arrangement of FIG. 2 is provided in place of each of the multipliers

FIG. 5 shows an optimization of the arrangement of FIG. 3; FIG. 6 shows the order of operations in the arrangements of FIGS. 2-5;

FIG. 7 shows the order of operations in accordance with embodiments of the present invention;

FIG. 8 shows a circuit arrangement in accordance with an

FIG. 9 is a cross-sectional view of a magnetic data storage medium encoded with a set of machine-executable instructions for performing a method according to the present invention:

FIG. 10 is a cross-sectional view of an optically readable data storage medium encoded with a set of machine executable instructions for performing a method according to the present invention;

FIG. 11 is a simplified block diagram of an illustrative system employing a programmable logic device incorporating the present invention; and

FIG. 12 is a flow diagram of an example of a method according to an embodiment of the present invention.

### DETAILED DESCRIPTION OF THE INVENTION

One example of the use of embodiments of the current invention is the evaluation of Galois Field (or finite field) polynomials. When large Galois Field multiplier arrays (such as those used for a Chien search in Flash memory errorcorrecting codes, including BCH and Reed-Solomon codes) are used, the performance on an FPGA is greatly reduced because of the depth of logic. If the calculation is pipelined, the resource count increases significantly because of inefficiencies of packing the partial product calculations into LUTs effectively.

According to embodiments of the current invention, a Galois Field polynomial may be mapped in a new way onto FPGA logic structures. These embodiments can be used to quickly and efficiently evaluate polynomials for such applications such as the aforementioned Chien search used by BCH and Reed Solomon decoders. System performance requirements may require that these structures operate at speeds over 300 MHz, which may not be possible with previously known polynomial structures for FPGAs, particularly for some BCH applications that use larger field sizes (e.g.,

A Chien search of polynomials requires one finite field multiplier for each polynomial term. If more than one location is checked at a time, the polynomial can be shifted to check another location by simply shifting each polynomial term. Shifting of the polynomial terms can be accomplished by multiplying each term with the required finite field value in multipliers 101, and summing all of the multiplier outputs together in adder 102, as shown in the arrangement in FIG. 1, in which the an terms are Galois Field elements that represent powers of the roots of the field, and the Xn terms are Galois

Field elements that represent terms of the error locator polynomial (i.e., the polynomial being searched).

Each finite field multiplier 101 may have the structure 200 shown in FIG. 2, in which there are m partial products 201 having m bits each, where m is the number of bits in the field. Each respective partial product may be generated by ANDing the  $\lambda_n$  input with a respective bit of the an input, as shown in the example of FIG. 3, which shows example of a 4-bit polynomial term ( $\lambda$ ) and one bit of a root powers value ( $\alpha$ ) generating one 4-bit partial product (in this case m=4). Each partial product is left shifted (211) by the bit position index of the bit in the second input to which it corresponds. The partial products are all summed in adder 202, creating a value having 2m-1 bits. That number is then reduced back to m-bits at 203 using the irreducible polynomial for the field, according to any of various known reduction techniques.

Thus, the arrangement of FIG. 1 may have the structure 400 shown in FIG. 4, with each multiplier 101 replaced with a copy of structure 200. One way to improve the efficiency of 20 structure 400 is to eliminate the individual reducers 203, add the outputs of the various adders 202 in a further adder 502, and then apply a single reduction 503, as shown in FIG. 5, and as described in copending, commonly-assigned U.S. patent application Ser. No. 12/719,770, which is hereby incorporated by reference herein in its entirety.

However, even with the structure of FIG. 5, adding together all of the partial products still creates a potentially large number of values each having 2m-1 bits. This may create a very long logic path from the input finite field numbers  $\alpha, \lambda$  to 30 the output of the result. And if pipelining is used (by cutting the paths at any point, whether within or between the individual multipliers), the logic size may increase significantly, because of the uneven packing of the relatively shifted partial product bits into the LUTs, which increases as pipelining 35 depth increases.

A solution in accordance with embodiments of the invention may be appreciated after considering FIGS. 6 and 7.

FIG. **6** is a diagrammatic representation of the matrix **600** of operations performed by arrangements such as that of the 40 circuit arrangement of FIG. **5**. Each multiplier is represented by a column **601**. There are (n-k)/2 multipliers, corresponding to the number of columns, where n is the number of bits (for BCH coding) or symbols (for Reed-Solomon coding) in the codeword, and k is the number of data bits or symbols in 45 the codeword—i.e., (n-k) is the number of parity bits or symbols in the codeword. There are m partial product generators **602** per multiplier, each m bits wide. Relative shifts are not shown. As indicated by arrow **603**, the direction of first addition, corresponding to adders **202**, is downward.

It can be shown mathematically that the identical result would be obtained if, as in matrix 700 of FIG. 7, the direction of first addition were horizontal as indicated by arrow 701. This may be implemented, as one example, by the circuit arrangement 750 of FIG. 8.

In arrangement 750, each column 601 of partial products 602 still represents a single term of the polynomial being evaluated (the relative shifts are shown in this drawing). However, unlike in arrangement 500, the partial products 602 in each of columns 601 are not added together in this case. 60 Instead, the partial products 602 in each of rows 751 are added first. As shown here, this may be accomplished with a respective adder 752. It will be appreciated that while the adders 752 are shown as being logically located in each respective row 751 between each respective column 601, they may physically be present in those locations, but they also may be elsewhere on the programmable integrated circuit device and

4

connected by routing resources of the programmable integrated circuit device to the respective partial product generators 602.

After all of the rows **751** have been added, the resulting sums **753**, which are aligned with respective 1-bit offsets **754** as shown, are added by adder **755**, and then reduced at **756** from 2m-1 bits to m bits. Because the additions of rows **751** occur prior to the offsetting or shifting, they can be efficiently packed into the LUTs of a programmable device. Therefore, even if the addition operations are pipelined (possible cut points where pipelining may occur are shown at dashed lines **702** of FIG. **7**), there will be minimal additional programmable logic of the programmable device required to complete the additions. Although the final addition **755** occurs after offsetting or shifting, it is only one operation, so any inefficiency introduced at that point also has minimal effect.

As noted above, when arrangement 750 is constructed in programmable logic, adders 752 may be located elsewhere than between the partial product generators 602. Indeed, both the partial product generators 602 and the adders 752 could be configured by a user completely from programmable logic resources along with programmable interconnect resources. As one alternative, separate dedicated multiplication circuits may be provided in hard-wired form on the programmable device and the user may use the programmable interconnect resources to create addition circuits and connect them to the dedicated multiplication circuits to form arrangement 750.

One example of a method 1200 for configuring a programmable device as circuitry for evaluating a polynomial in accordance with an embodiment of the present invention is diagrammed in FIG. 12. Method 1200 begins at 1201, where, on the programmable device, a respective partial product generator is configured for each bit position of each term of a plurality of terms of a polynomial to be evaluated. Next, at 1202, a respective plurality of adders is configured on the programmable device for each bit position, to add partial products of a respective bit position across all of the plurality of terms to provide a respective bit-slice sum, wherein resulting bit-slice sums are offset from one another according to their respective bit positions. Finally, at 1203, a final adder that adds together said respective offset bit-slice sums to provide a result is configured on the programmable device.

Thus it is seen that circuitry and methods for efficiently performing polynomial calculations have been provided.

Instructions for carrying out a method according to this invention for programming a programmable device to perform polynomial calculations, may be encoded on a machine-readable medium, to be executed by a suitable computer or similar device to implement the method of the invention for programming or configuring PLDs or other programmable devices to perform operations as described above. For example, a personal computer may be equipped with an interface to which a PLD can be connected, and the personal computer can be used by a user to program the PLD using a suitable software tool, such as the QUARTUS® II software available from Altera Corporation, of San Jose, Calif.

FIG. 9 presents a cross section of a magnetic data storage medium 800 which can be encoded with a machine executable program that can be carried out by systems such as the aforementioned personal computer, or other computer or similar device. Medium 800 can be a floppy diskette or hard disk, or magnetic tape, having a suitable substrate 801, which may be conventional, and a suitable coating 802, which may be conventional, on one or both sides, containing magnetic domains (not visible) whose polarity or orientation can be altered magnetically. Except in the case where it is magnetic

tape, medium 800 may also have an opening (not shown) for receiving the spindle of a disk drive or other data storage device

The magnetic domains of coating **802** of medium **800** are polarized or oriented so as to encode, in manner which may be 5 conventional, a machine-executable program, for execution by a programming system such as a personal computer or other computer or similar system, having a socket or peripheral attachment into which the PLD to be programmed may be inserted, to configure appropriate portions of the PLD, 10 including its specialized processing blocks, if any, in accordance with the invention.

FIG. 10 shows a cross section of an optically-readable data storage medium 810 which also can be encoded with such a machine-executable program, which can be carried out by 15 systems such as the aforementioned personal computer, or other computer or similar device. Medium 810 can be a conventional compact disk read-only memory (CD-ROM) or digital video disk read-only memory (DVD-ROM) or a rewriteable medium such as a CD-R, CD-RW, DVD-R, DVD-RW, DVD+RW, or DVD-RAM or a magneto-optical disk which is optically readable and magneto-optically rewriteable. Medium 810 preferably has a suitable substrate 811, which may be conventional, and a suitable coating 812, which may be conventional, usually on one or both sides of 25 substrate 811.

In the case of a CD-based or DVD-based medium, as is well known, coating **812** is reflective and is impressed with a plurality of pits **813**, arranged on one or more layers, to encode the machine-executable program. The arrangement of 30 pits is read by reflecting laser light off the surface of coating **812**. A protective coating **814**, which preferably is substantially transparent, is provided on top of coating **812**.

In the case of magneto-optical disk, as is well known, coating **812** has no pits **813**, but has a plurality of magnetic 35 domains whose polarity or orientation can be changed magnetically when heated above a certain temperature, as by a laser (not shown). The orientation of the domains can be read by measuring the polarization of laser light reflected from coating **812**. The arrangement of the domains encodes the 40 program as described above.

A PLD 90 programmed according to the present invention may be used in many kinds of electronic devices. One possible use is in a data processing system 900 shown in FIG. 11. Data processing system 900 may include one or more of the 45 following components: a processor 901; memory 902; I/O circuitry 903; and peripheral devices 904. These components are coupled together by a system bus 905 and are populated on a circuit board 906 which is contained in an end-user system 907.

System 900 can be used in a wide variety of applications, such as computer networking, data networking, instrumentation, video processing, digital signal processing, or any other application where the advantage of using programmable or reprogrammable logic is desirable. PLD 90 can be used to 55 perform a variety of different logic functions. For example, PLD 90 can be configured as a processor or controller that works in cooperation with processor 901. PLD 90 may also be used as an arbiter for arbitrating access to a shared resources in system 900. In yet another example, PLD 90 can be configured as an interface between processor 901 and one of the other components in system 900. It should be noted that system 900 is only exemplary, and that the true scope and spirit of the invention should be indicated by the following claims.

Various technologies can be used to implement PLDs 90 as described above and incorporating this invention.

6

It will be understood that the foregoing is only illustrative of the principles of the invention, and that various modifications can be made by those skilled in the art without departing from the scope and spirit of the invention. For example, the various elements of this invention can be provided on a PLD in any desired number and/or arrangement. One skilled in the art will appreciate that the present invention can be practiced by other than the described embodiments, which are presented for purposes of illustration and not of limitation, and the present invention is limited only by the claims that follow.

What is claimed is:

1. Polynomial circuitry for evaluating a polynomial having a plurality of terms, each term having a number of bit positions, said polynomial circuitry comprising:

- a plurality of groups of partial product generators, each of said groups of partial product generators corresponding to a single term in said plurality of terms and, in each one of said groups of partial product generators, each respective partial product generator in said one of said groups of partial product generators providing an output value for a respective single input bit position of said single term to which said one of said groups of partial product generators corresponds;
- adder circuitry for providing respective bit-slice sums, said adder circuitry comprising a plurality of respective groups of adders, each respective group of adders in said plurality of respective groups of adders including a number of adders equal in number to said plurality of terms and corresponding to one respective bit position in all of said plurality of terms, and summing output values of multiple ones of said partial product generators for said one respective bit position to provide said respective bit-slice sum having a respective bit-width, wherein resulting bit-slice sums are offset from one another, by less than their respective bit-widths, according to their respective bit positions, said plurality of groups of adders being equal in number to said number of bit positions; and
- a final adder that adds together said respective offset bitslice sums to provide a final result.
- 2. The polynomial circuitry of claim 1 wherein: said terms have m bit positions; and each respective partial product generator provides a partial result that is m bits wide.
- 3. The polynomial circuitry of claim 2 further comprising reduction circuitry that reduces width of said final result to m bits
- 4. The polynomial circuitry of claim 1 further comprising reduction circuitry that reduces bit width of said final result.
- 5. The polynomial circuitry of claim 1 wherein each adder of said plurality of respective groups of adders is configured using at least one look-up table of a programmable integrated circuit device.
- **6**. The polynomial circuitry of claim **5** wherein said programmable integrated circuit device comprises a field-programmable gate array.
- 7. A method of configuring a programmable device as circuitry for evaluating a polynomial having a plurality of terms, each term having a number of bit positions, said 60 method comprising:
  - configuring, on said programmable device, a plurality of groups of partial product generators, each of said groups of partial product generators corresponding to a single term in said plurality of terms and, in each one of said groups of partial product generators, each respective partial product generator in said one of said groups of partial product generators providing an output value for

a respective single input bit position of said single term to which said one of said groups of partial product generators corresponds;

configuring, on said programmable device, adder circuitry for providing respective bit-slice sums, said adder cir- 5 cuitry comprising a plurality of respective groups of adders, each respective group of adders in said plurality of respective groups of adders including a number of adders equal in number to said plurality of terms and corresponding to one respective bit position in all of said plurality of terms, and summing output values of multiple ones of said partial product generators for said one respective bit position to provide said respective bitslice sum having a respective bit-width, wherein resulting bit-slice sums are offset from one another, by less 15 than their respective bit-widths, according to their respective bit positions, said plurality of groups of adders being equal in number to said number of bit positions; and

configuring, on said programmable device, a final adder 20 that adds together said respective offset bit-slice sums to provide a final result.

8. The method of claim 7 wherein:

said terms have m bit positions; and

said configuring a plurality of partial product generators 25 comprises configuring each partial product generator to provide a partial result that is m bits wide.

- **9.** The method of claim **8** further comprising configuring, on said programmable device, reduction circuitry that reduces width of said final result to m bits.
- 10. The method of claim 7 further comprising configuring, on said programmable device, reduction circuitry that reduces bit width of said final result.
- 11. The method of claim 7 wherein configuring adder circuitry comprises configuring each adder of said respective 35 groups of adders using at least one look-up table of a programmable integrated circuit device.
- 12. The method of claim 11 wherein configuring adder circuitry comprises configuring each adder of said respective groups of adders using at least one look-up table of a field- 40 programmable gate array.
- 13. A non-transitory machine-readable data storage medium encoded with non-transitory machine-executable instructions for configuring a programmable device as circuitry for evaluating a polynomial having a plurality of terms, 45 each term having a number of bit positions, said instructions comprising:

instructions to configure, on said programmable device, a plurality of groups of partial product generators, each of said groups of partial product generators corresponding 50 to a single term in said plurality of terms and, in each one

8

of said groups of partial product generators, each respective partial product generator in said one of said groups of partial product generators providing an output value for a respective single input bit position of said single term to which said one of said groups of partial product generators corresponds;

instructions to configure, on said programmable device. adder circuitry for providing respective bit-slice sums, said adder circuitry comprising a plurality of respective groups of adders, each respective group of adders in said plurality of respective groups of adders including a number of adders equal in number to said plurality of terms and corresponding to one respective bit position in all of said plurality of terms, and summing output values of multiple ones of said partial product generators for said one respective bit position to provide said respective bit-slice sum having a respective bit-width, wherein resulting bit-slice sums are offset from one another, by less than their respective bit-widths, according to their respective bit positions, said plurality of groups of adders being equal in number to said number of bit positions; and

instructions to configure, on said programmable device, a final adder that adds together said respective offset bitslice sums to provide a final result.

14. The non-transitory machine-readable data storage medium of claim 13 wherein:

said terms have m bit positions; and

said instructions to configure a plurality of partial product generators comprises configuring each partial product generator to provide a partial result that is m bits wide.

- 15. The non-transitory machine-readable data storage medium of claim 14 further comprising instructions to configure, on said programmable device, reduction circuitry that reduces width of said final result to m bits.
- 16. The non-transitory machine-readable data storage medium of claim 13 further comprising instructions to configure, on said programmable device, reduction circuitry that reduces bit width of said final result.
- 17. The non-transitory machine-readable data storage medium of claim 13 wherein said instructions to configure adder circuitry comprise instructions to configure each adder of said respective groups of adders using at least one look-up table of a programmable integrated circuit device.
- 18. The non-transitory machine-readable data storage medium of claim 17 wherein said instructions to configure adder circuitry comprise instructions to configure each adder of said respective groups of adders using at least one look-up table of a field-programmable gate array.

\* \* \* \* \*